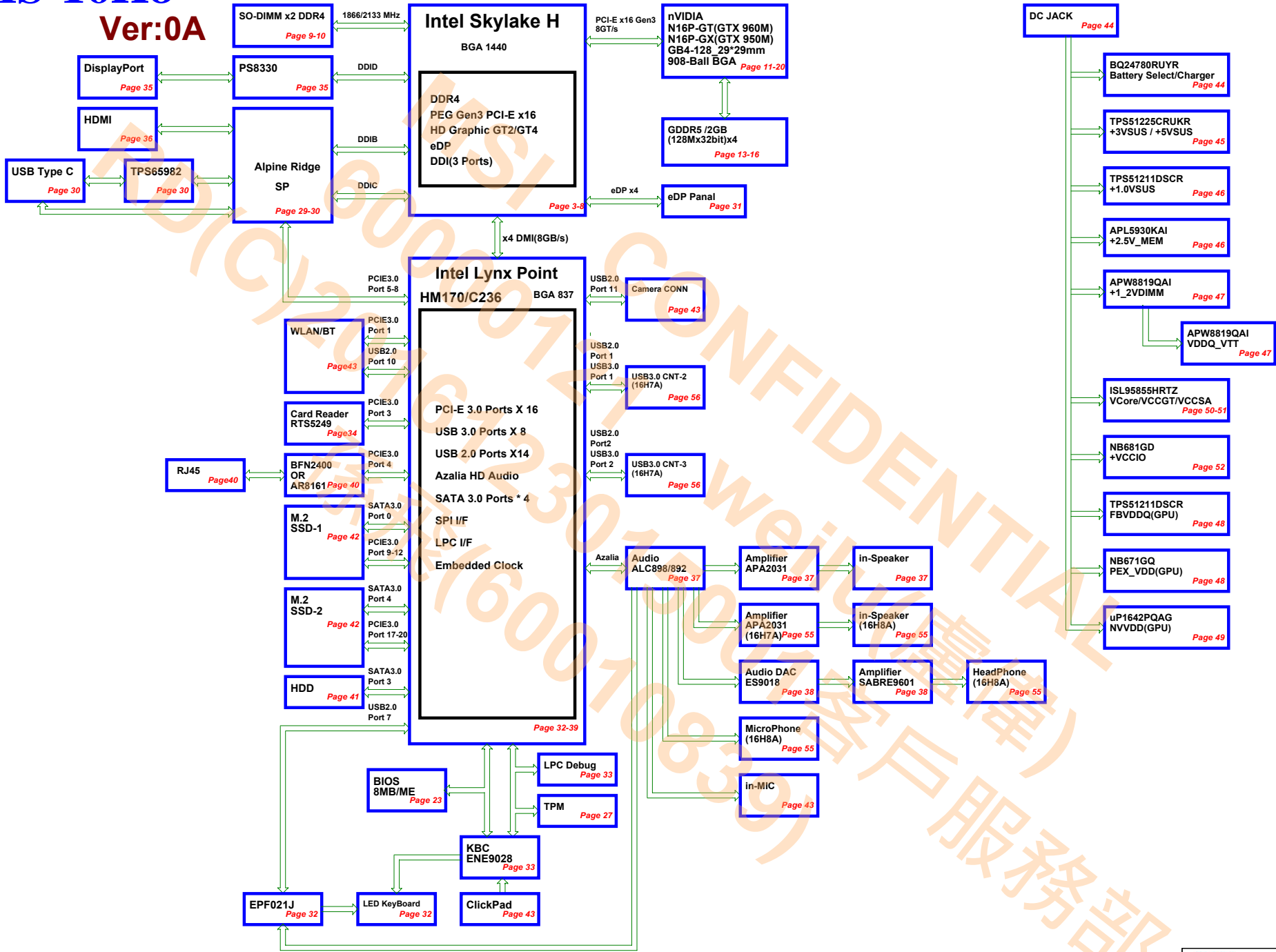
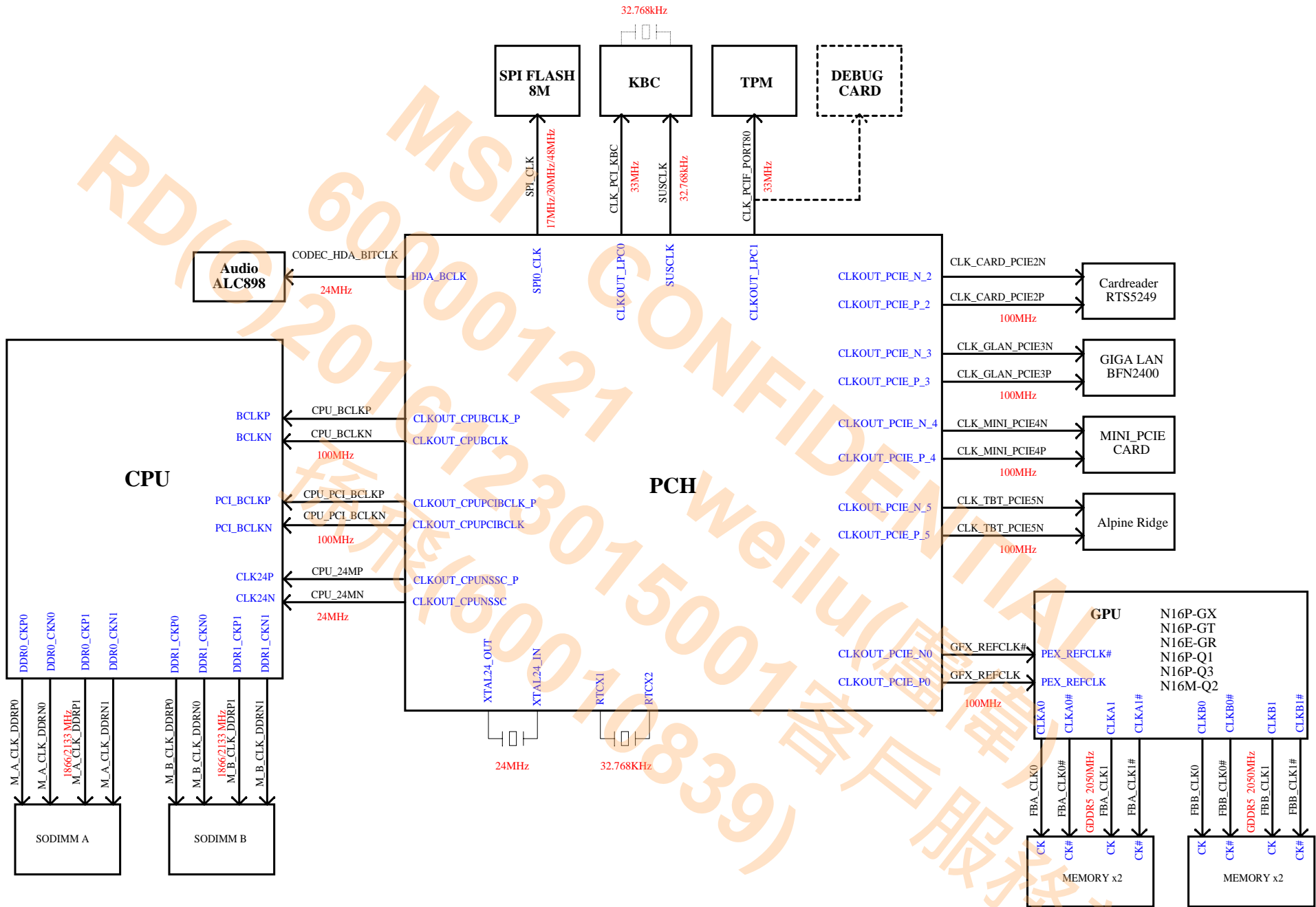


MS-16H8

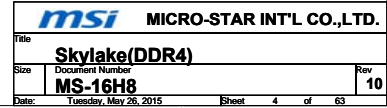
Ver:0A

Intel Skylake Platform





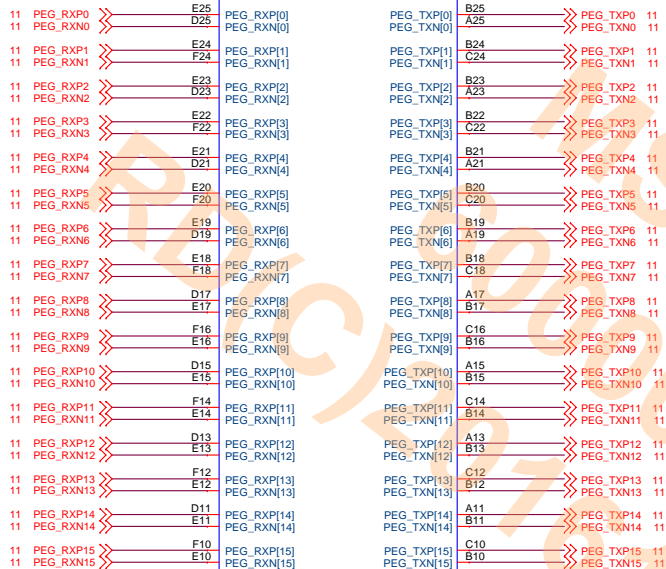
DDR Channel B



U3C SKYLAKE_HALO

BGA1440

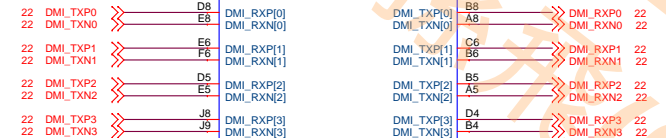
?



DDI B
DP

DDI C
HDMI

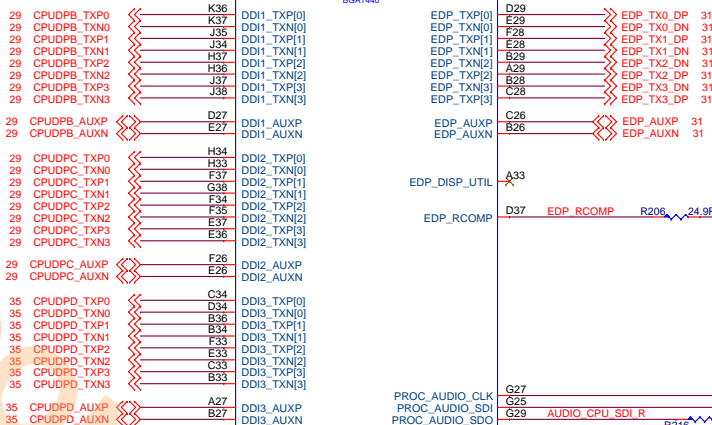
+VCCIO R37 24.9R1%0402 PEG_COMP G2 PEG_RCOMP



SKL_H_BGA_BGA REV = 1 ? 3 OF 14

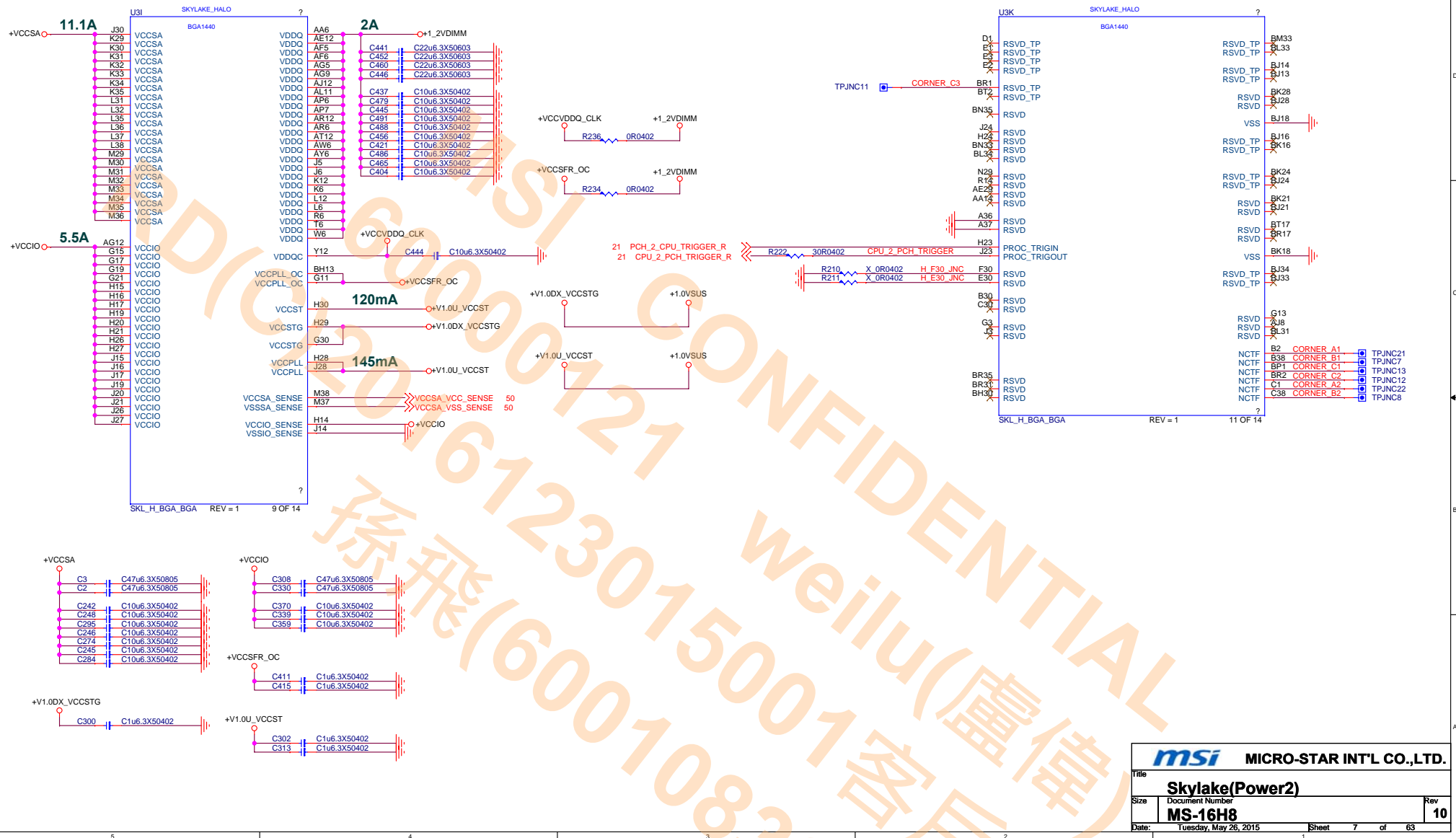
U3D SKYLAKE_HALO

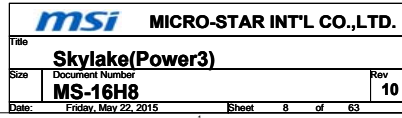
BGA1440



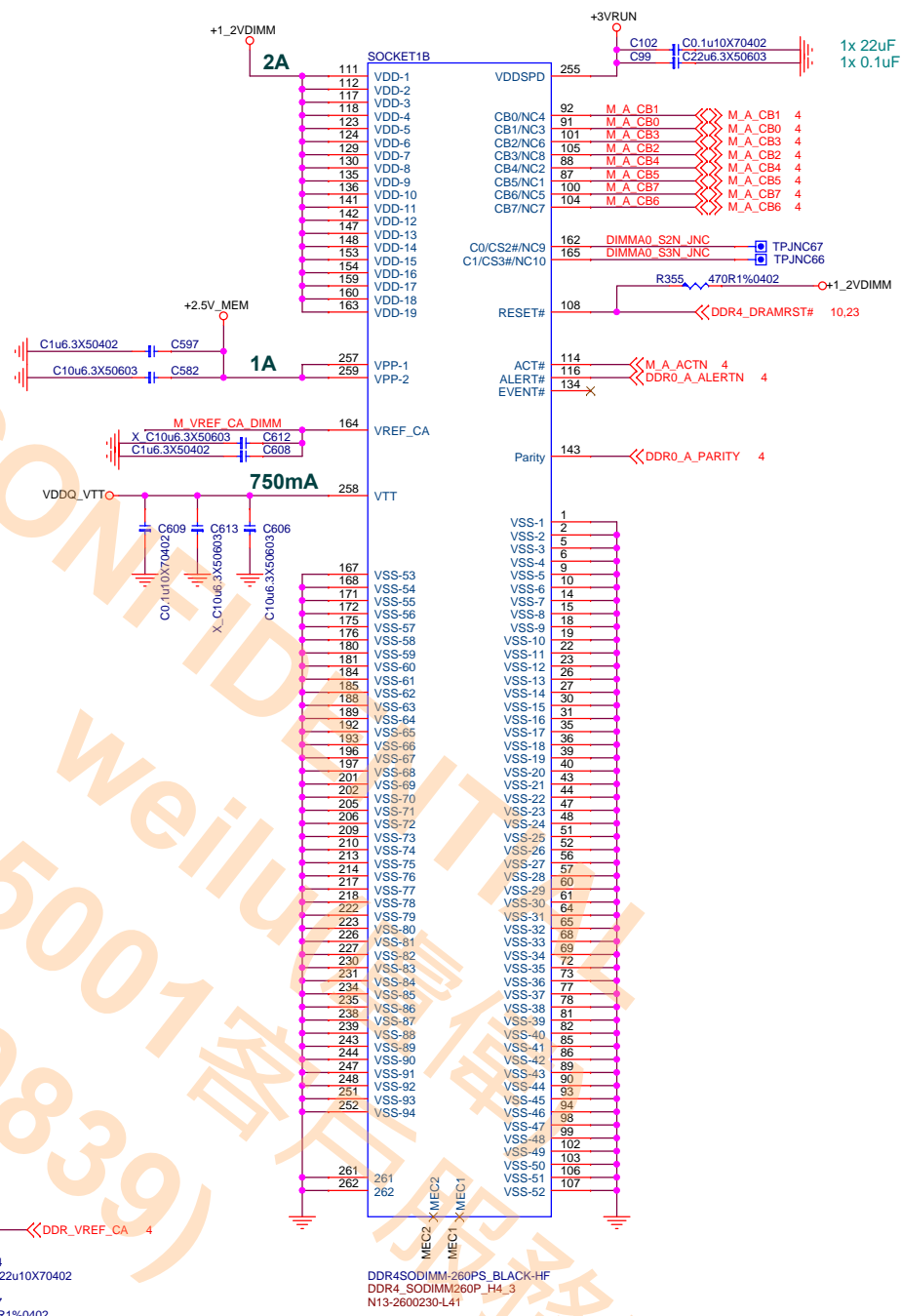
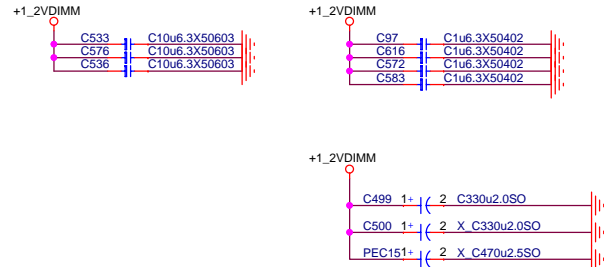
EDP

SKL_H_BGA_BGA REV = 1 ? 4 OF 14



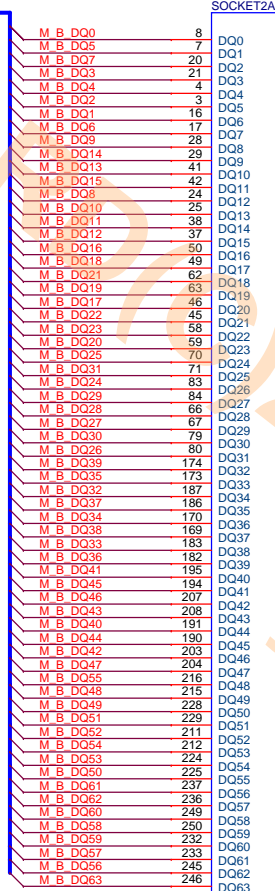


4 M A DQ[63:0] <<>

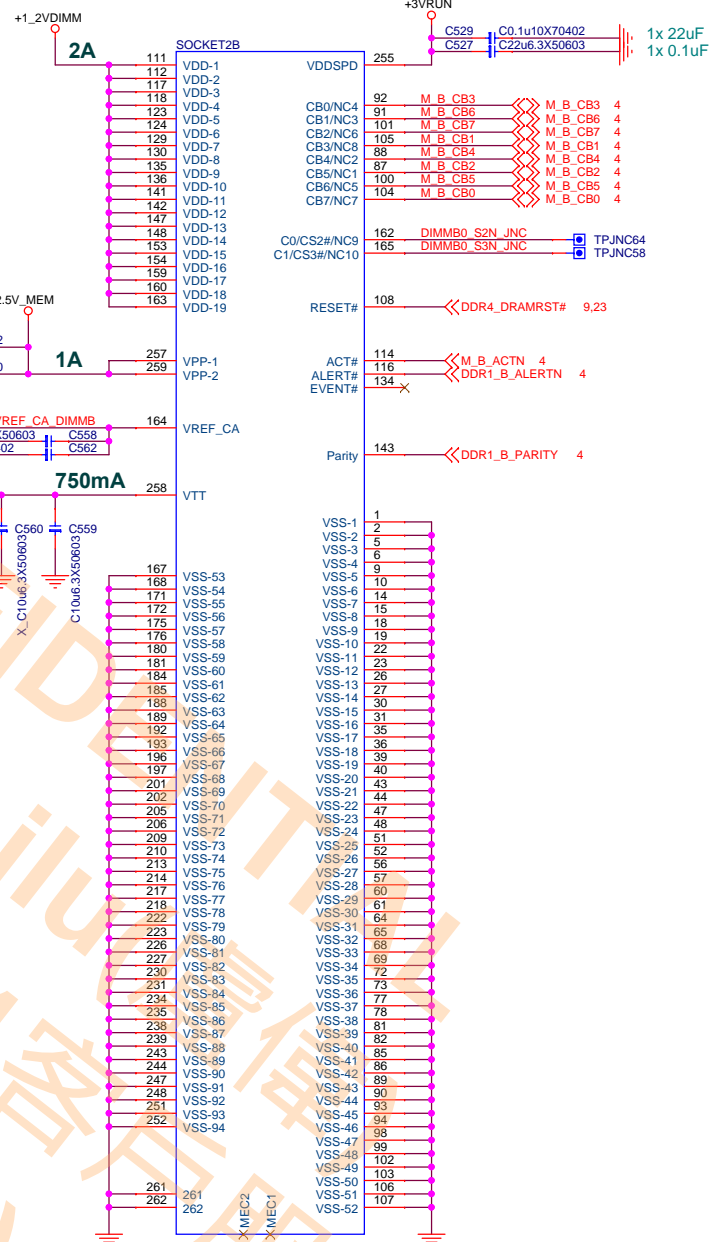
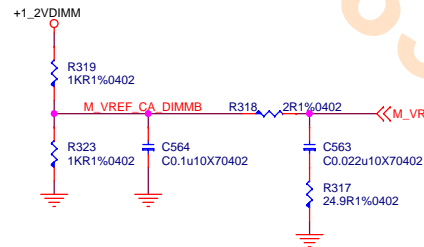
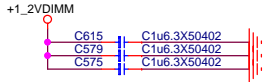
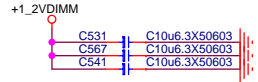


SODIMM_B0

4 M_B_DQ[63:0] <<>



DDR4SODIMM-260PS_BLACK-HF-1
DDR4_SODIMM260P_H4_2
N13-2600220-L41

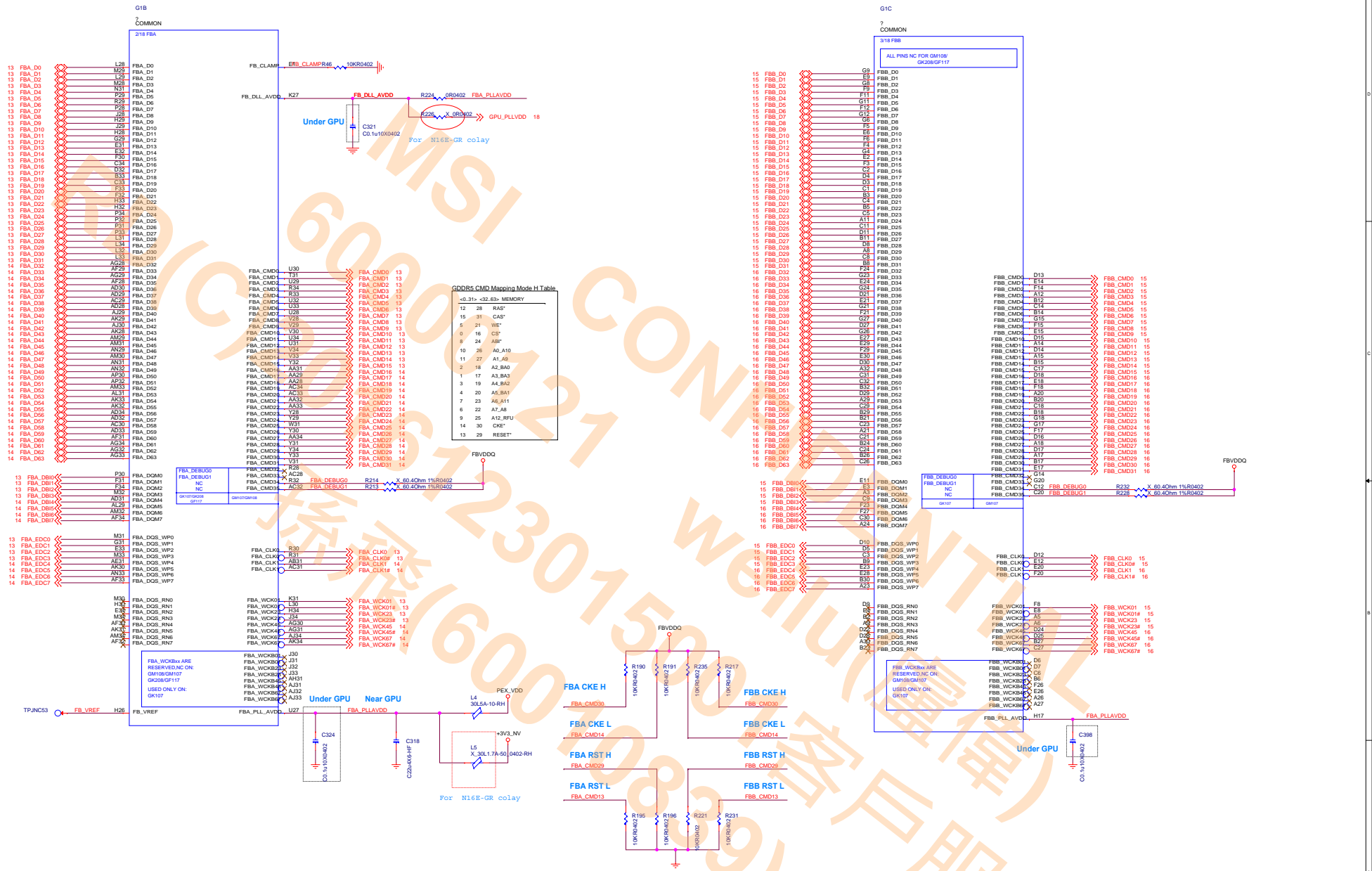


DDR4SODIMM-260PS_BLACK-HF-1
DDR4_SODIMM260P_H4_2
N13-2600220-L41

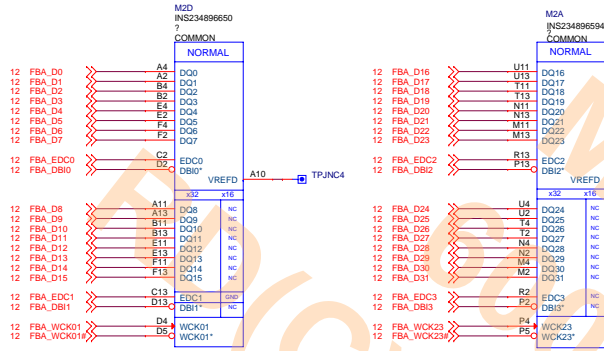
18,20,24,33 DGPU_PWRGD >> G N-2N7002LT1G_SOT23-RH
PEX_CLKREQ#



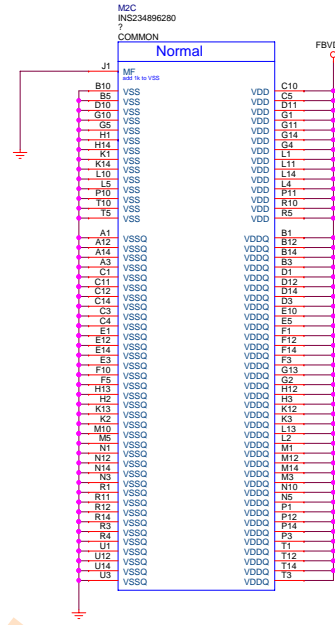
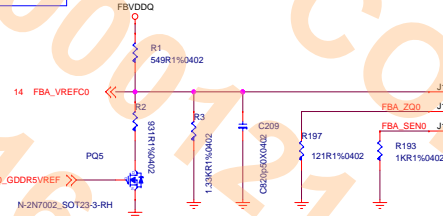
N16P-GX (Frame Buffer Interface)



N16P_GX(GDDR5 Frame A-1)

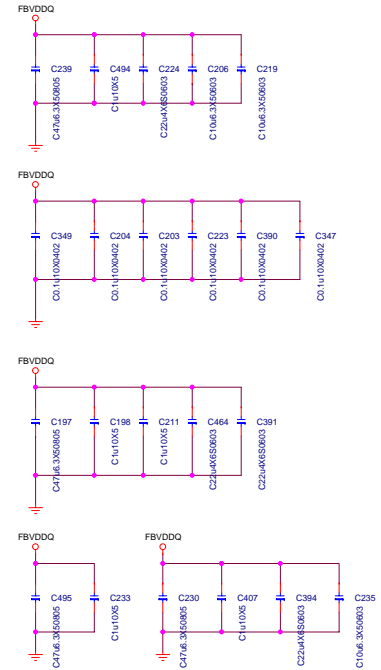
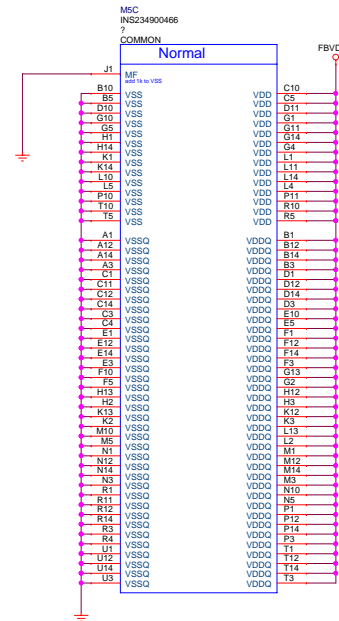
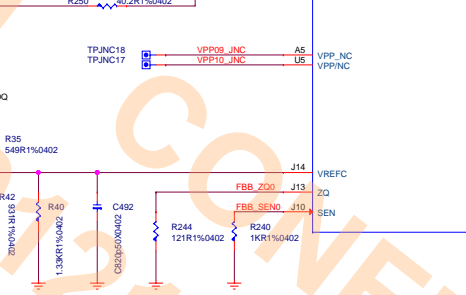
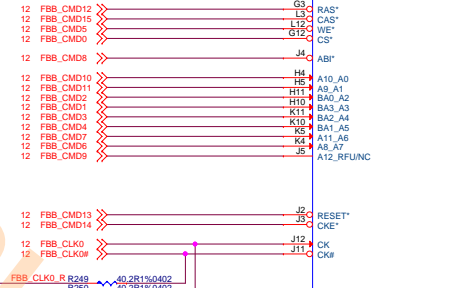
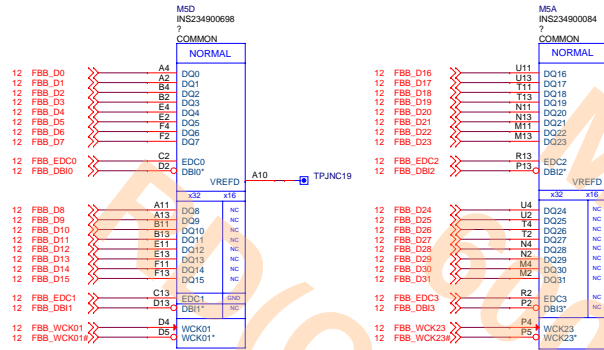


HVRAM
Hylix VRAM
M12-5GC2H05-H23

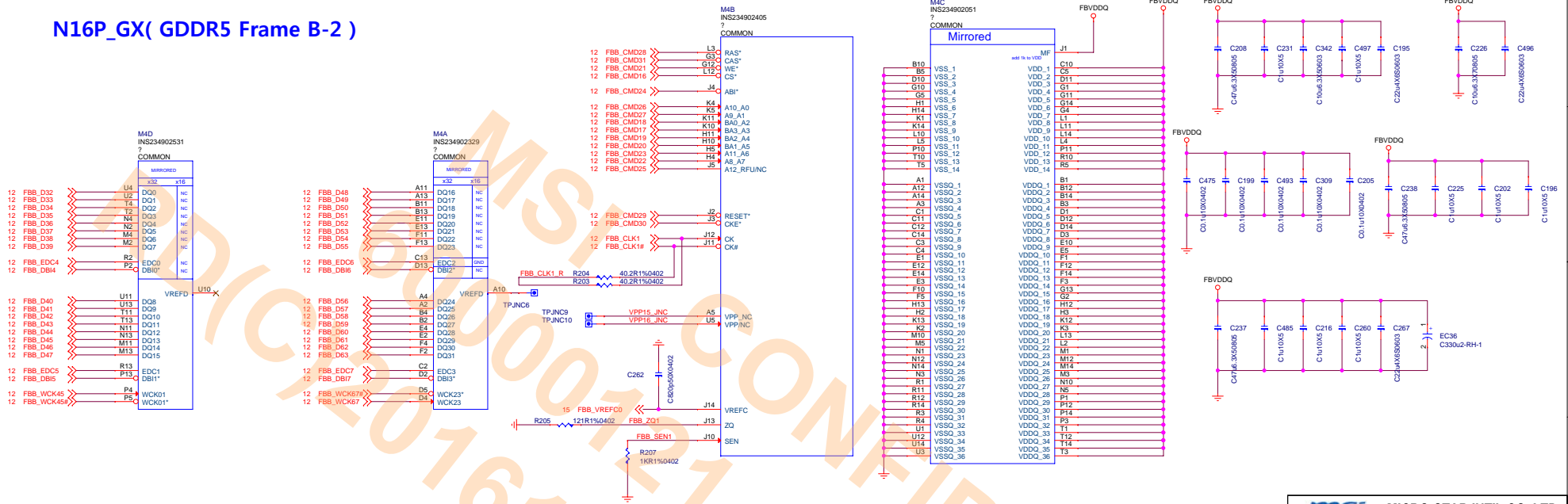




N16P_GX(GDDR5 Frame B-1)

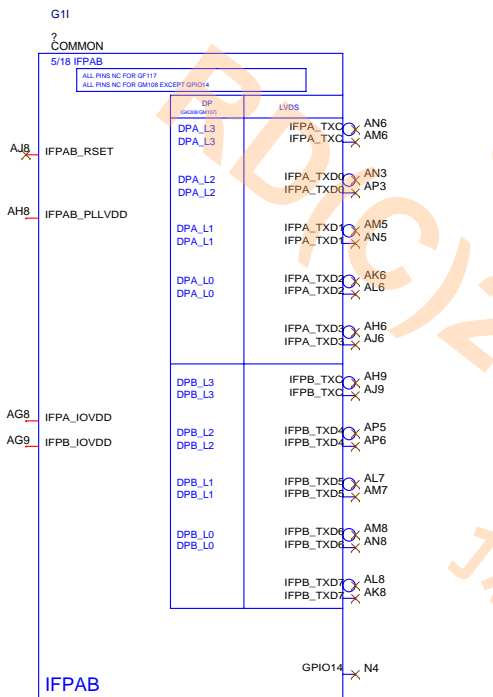


N16P_GX(GDDR5 Frame B-2)

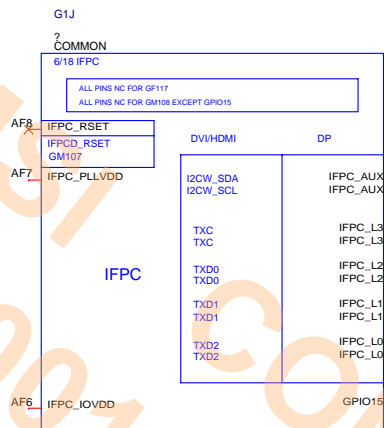


N16P-GX (Display IF)

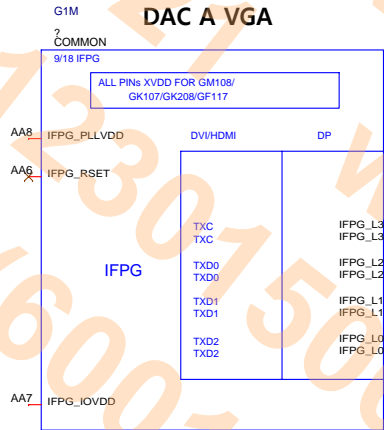
IFP A/B LVDSDual Link



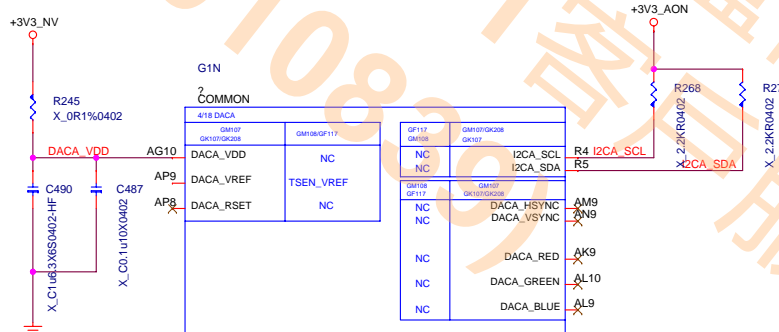
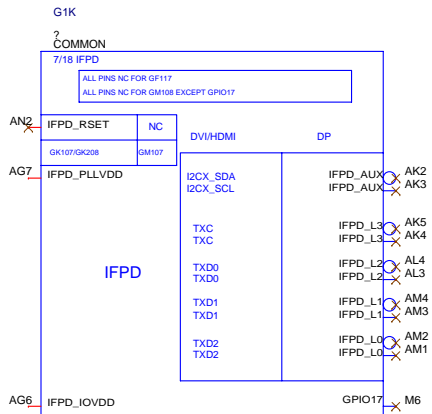
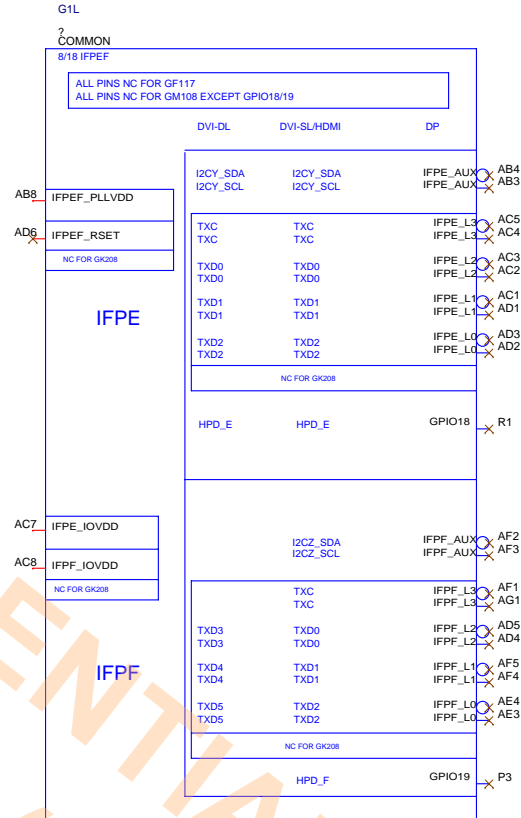
IFP C Native HDMI OR DP



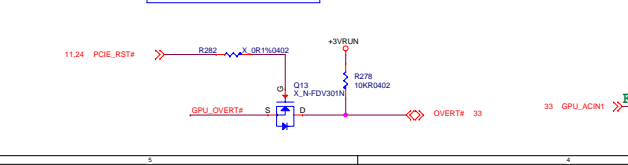
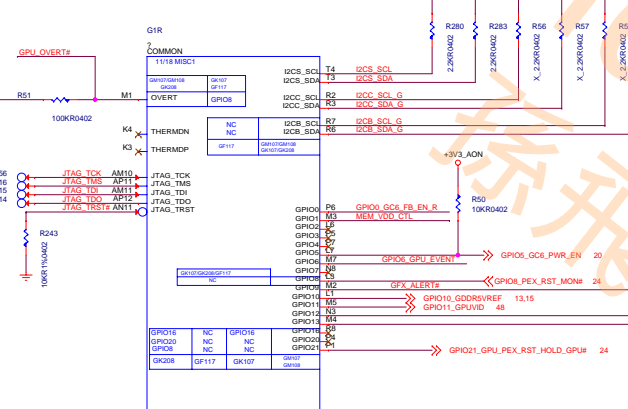
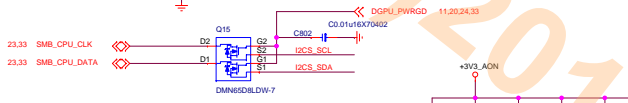
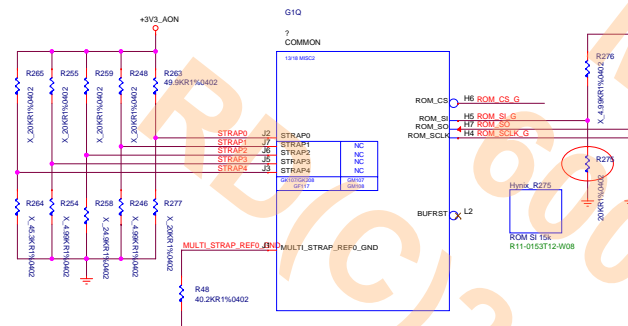
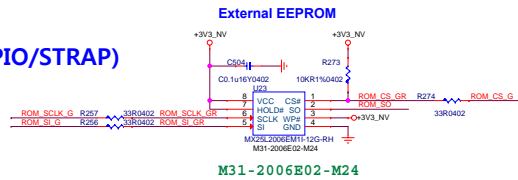
DAC A VGA



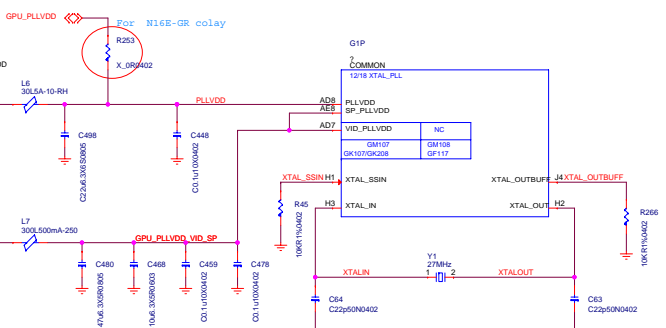
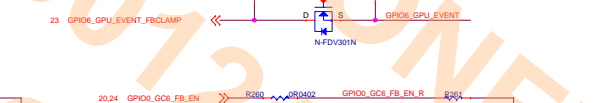
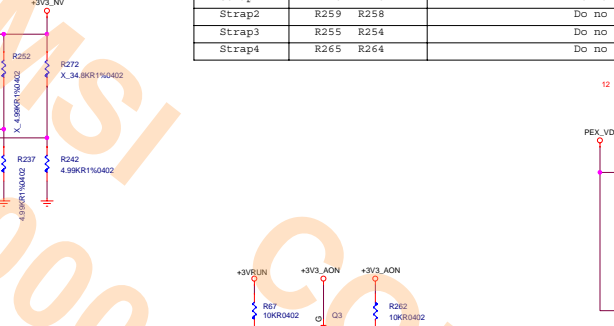
IFP E/F Dual Link TMDS DVI-I



N16P-GX (GPIO/STRAP)

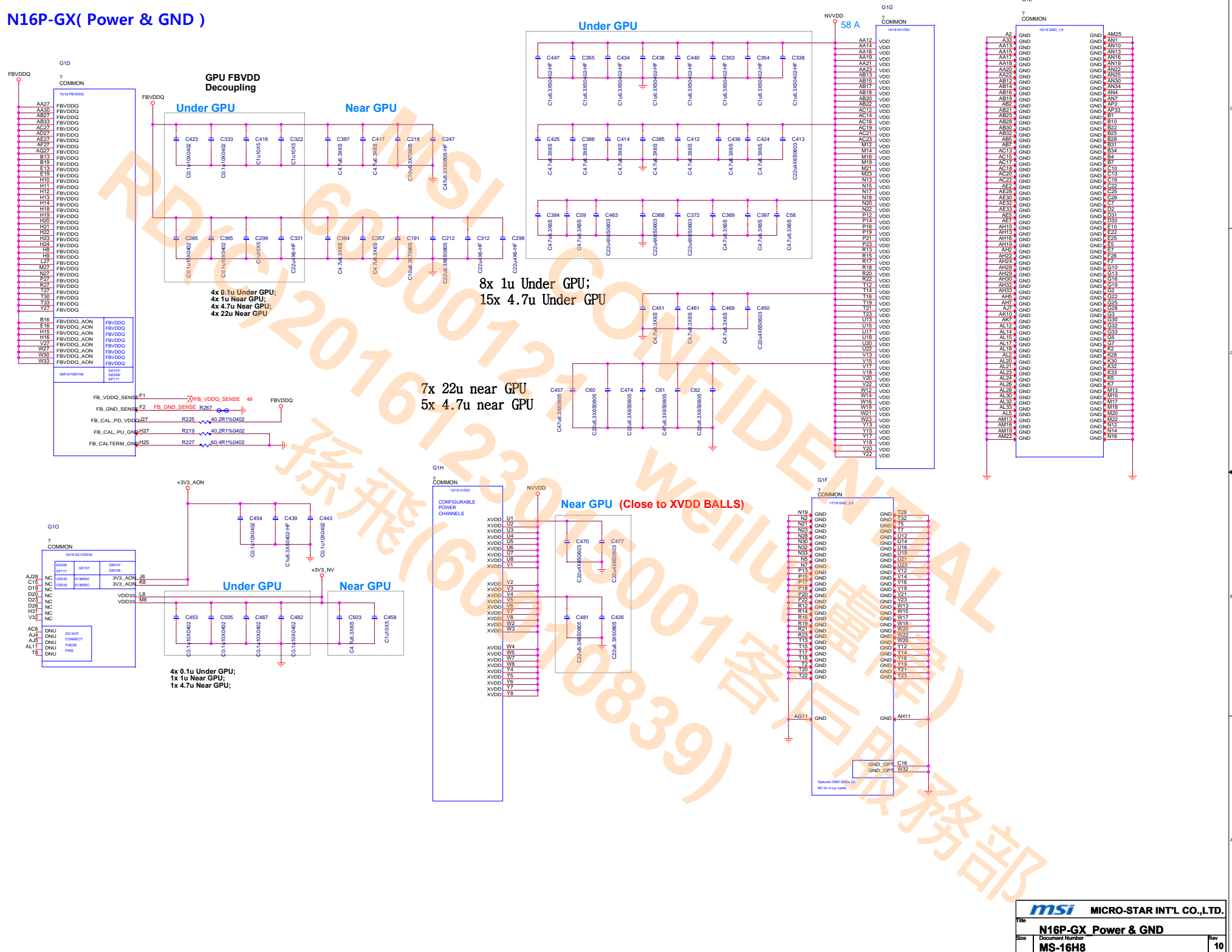


Item	Location	N16P-GX
Strap Mode	R48	MULTISTRAP_REF_GND,40.2K PD to GND
Device ID		0x0F84
Package		GB4B-128
Memory Type		GDDR5
ROM_S1	R275	0x2,Hynix 2G, 15kohm Pull Down H5GCA4H24MFR-T2C
	R275	0x3,Samsung 2G, 20kohm Pull Down K4G41325FC-HC03
	R275	0x4,Micron 2G, 24.9kohm Pull Down EDW4032BA8G-60-F
ROM_S0	R237	0x0,4.99kohm Pull Down
ROM_SCLK	R242	0x0,4.99kohm Pull Down
Strap0	R263	49.9kohm pull up to +3V3_AON
Strap1	R248 R246	Do no stuff
Strap2	R259 R258	Do no stuff
Strap3	R255 R254	Do no stuff
Strap4	R265 R264	Do no stuff



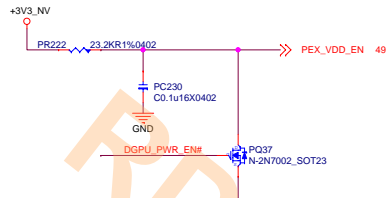
Pin Name	Normal function	I/O	Functional Description	
GP100	GC6_FB_EN	O	FB Enable GC62.0	10K PD
GP101	MEM_VDD_CTL	O	Memory Voltage Control	PU, PD to set
GP102	NC LCD_BL_PWM	O	Panel Backlight PWM	100K PD
GP103	NC LCD_PWR_EN	O	Panel power Enable	100K PD
GP104	NC LCD_BL_EN	O	Panel Backlight Enable	100K PD
GP105	GC6_PWR_EN	O	GPU Power Sequence for GC2.0	10K PU 3V3_AON
GP106	GPU_EVENT*	I	GPU Wake for GC2.0	10K PU 3V3_AON
GP107	NC Hstereo/Debug	O	3D Vision L/R Signal	100K PD
GP108	SYS_PEX_RST_MON*	I	SYS Side PCIe reset monitor	10K PU 3V3_AON
GP109	Therm_Alert*/ERR	I/O	Thermal ALERT	10K PU 3V3_AON
GP1010	GDDR5VREF	O	Memory VREF Control	100K PD
GP1011	GP1011_GPUVID	O	GPU Core VDD PWM control signal	
GP1012	GPU_ACIN	I	AC power detect	100K PU 3V3_AON
GP1013	FBVREF_PSI#	O	Phase Shedding	
GP1014	NC	I	Hot plug detect for IFPA	
GP1015	NC	I	Hot plug detect for IFPC	
GP1016	NC	O		
GP1017	NC	I	Hot plug detect for IFPD	
GP1018	NC	I	Hot plug detect for IFPE	
GP1019	NC	I	Hot plug detect for IFPF	
GP1021	SYS_PEX_RST_HOLD_GPU#	O	GPU PCIe self-reset contrl	10K PU 3V3_AON
OVER	OVERT	I/O	Catastrophic over temp	100K PU 3V3_AON

N16P-GX(Power & GND)

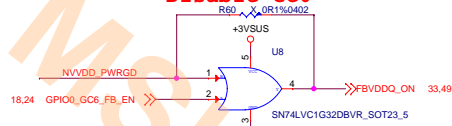


DGPU_Power Control

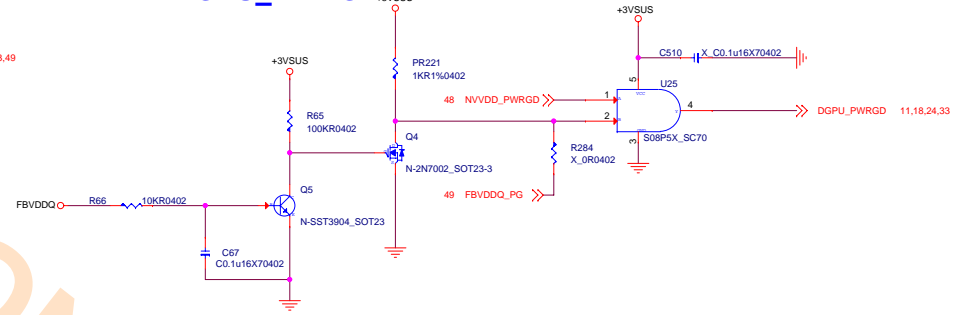
PEX_VDD_EN



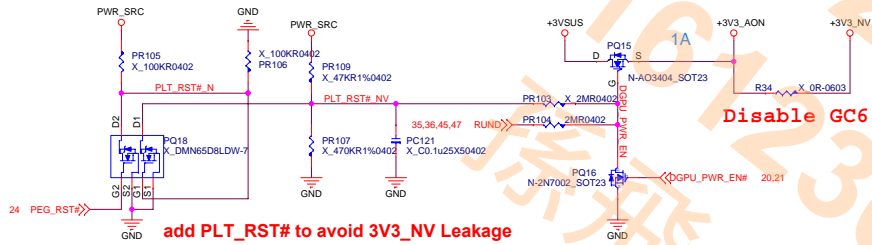
Disable GC6



DGPU_PWRGD

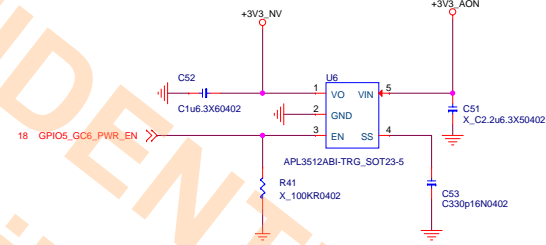


nVIDIA Power Sequence Control 3V3_NV -> NVDD, PEX_VDD -> FBVDDQ -> DGPUPWRGD

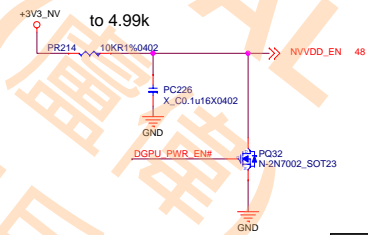
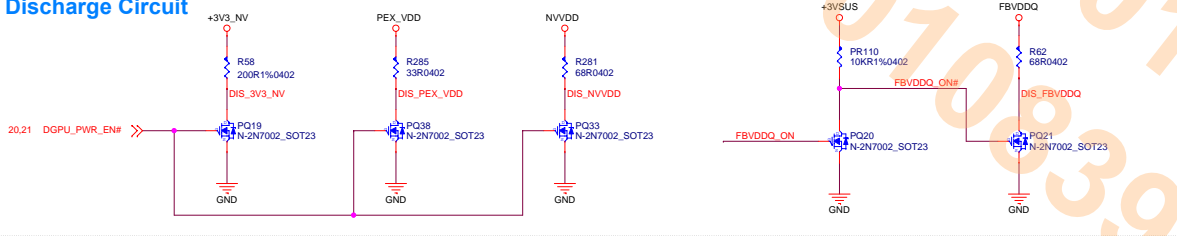


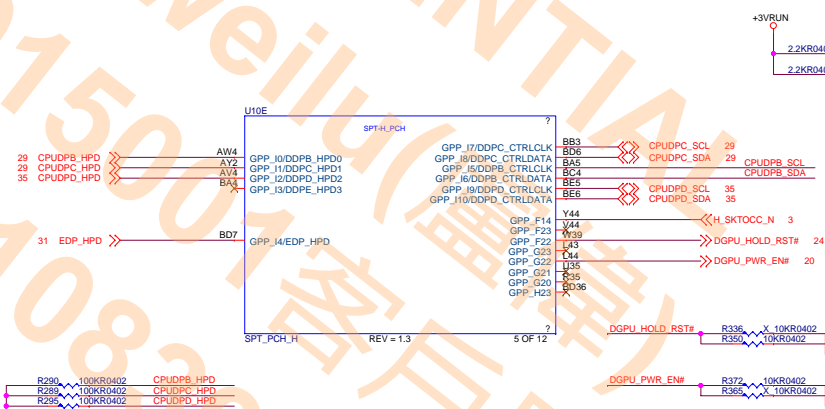
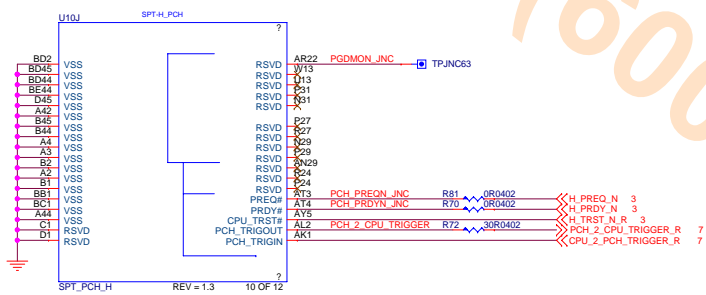
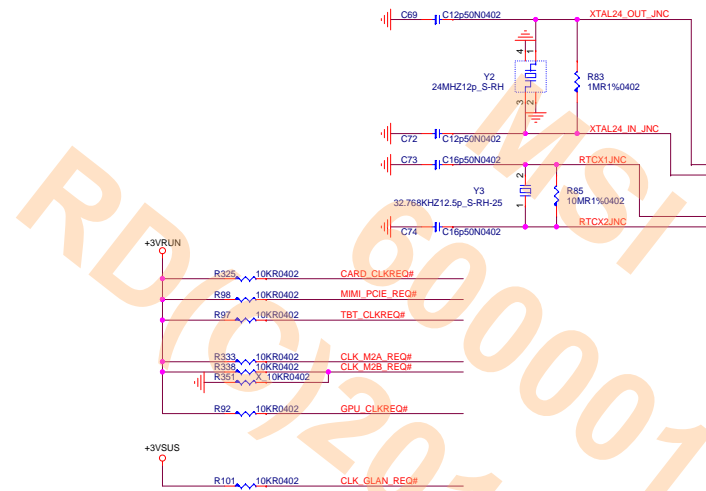
add PLT_RST# to avoid 3V3_NV Leakage

Disable GC6



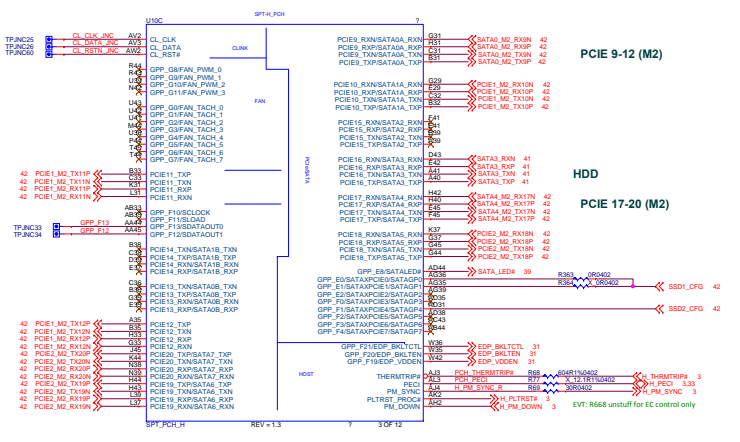
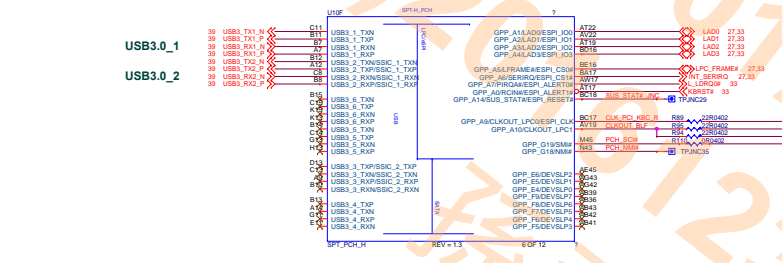
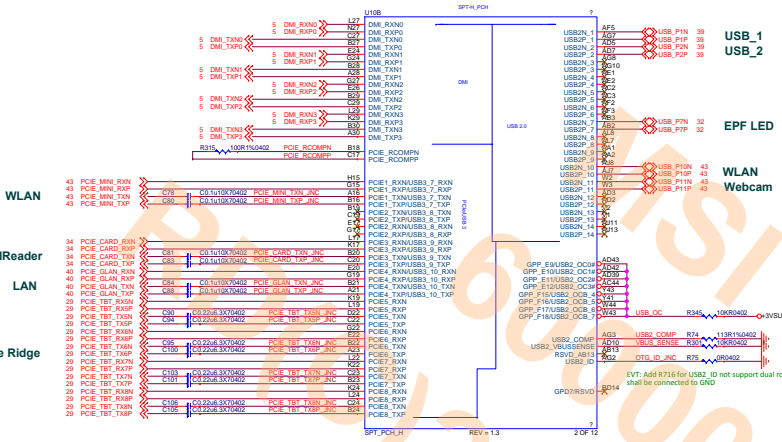
Discharge Circuit



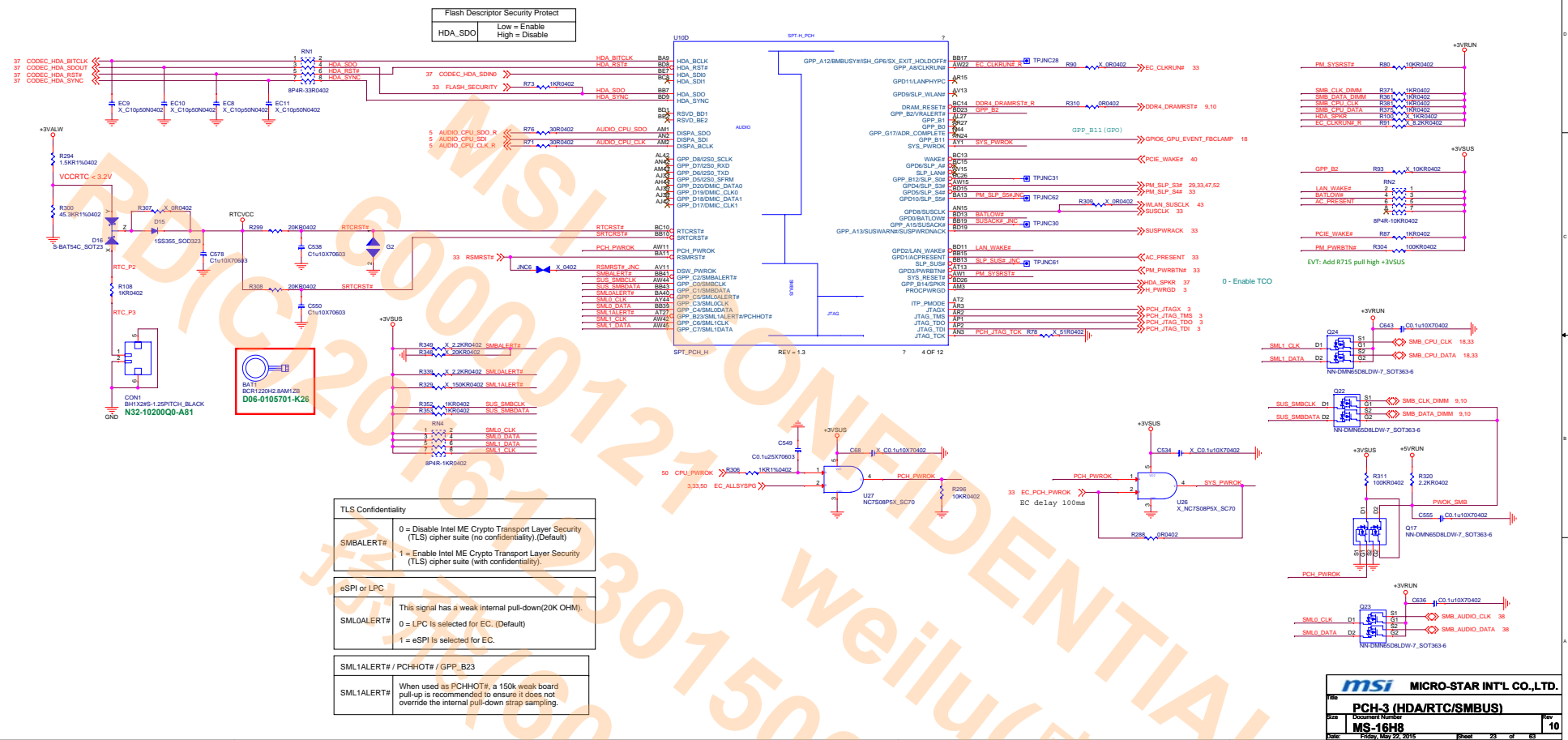


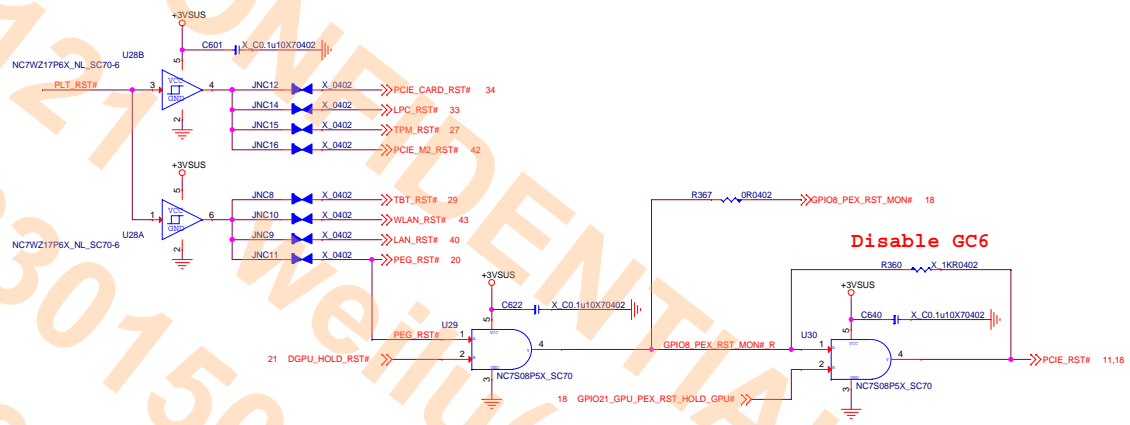
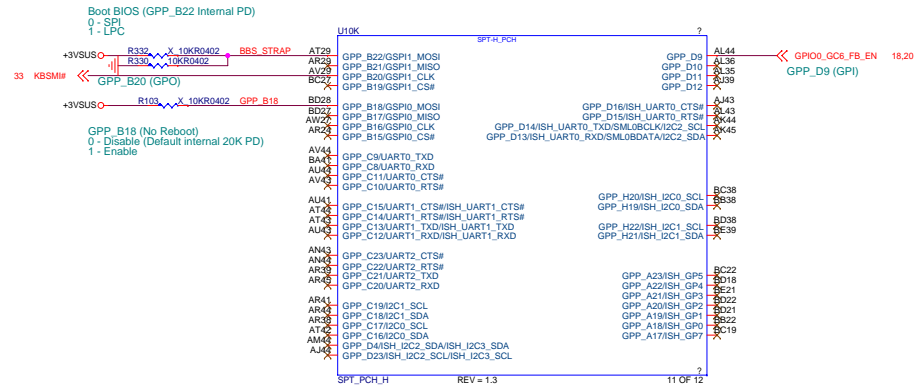
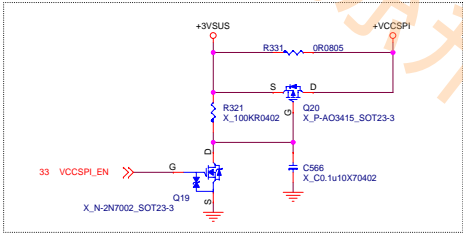
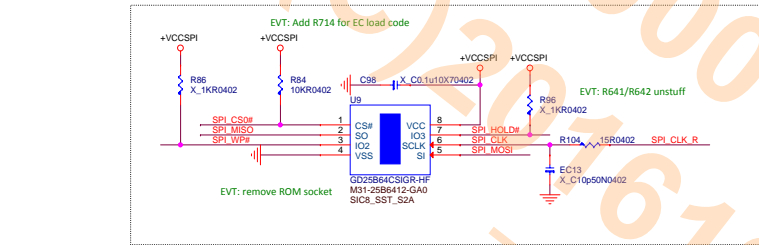
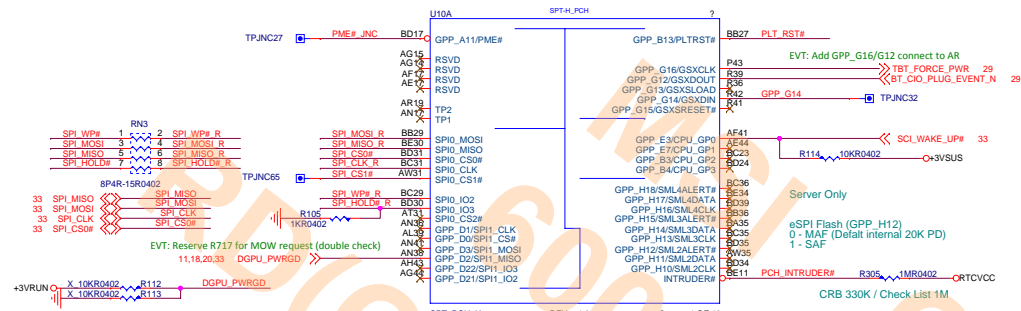
Signal	GPIO Assignment
DGPU_PWR_EN#	GPP_G22
DGPU_PWROK	NA
DGPU_HOLD_RST#	GPP_F22

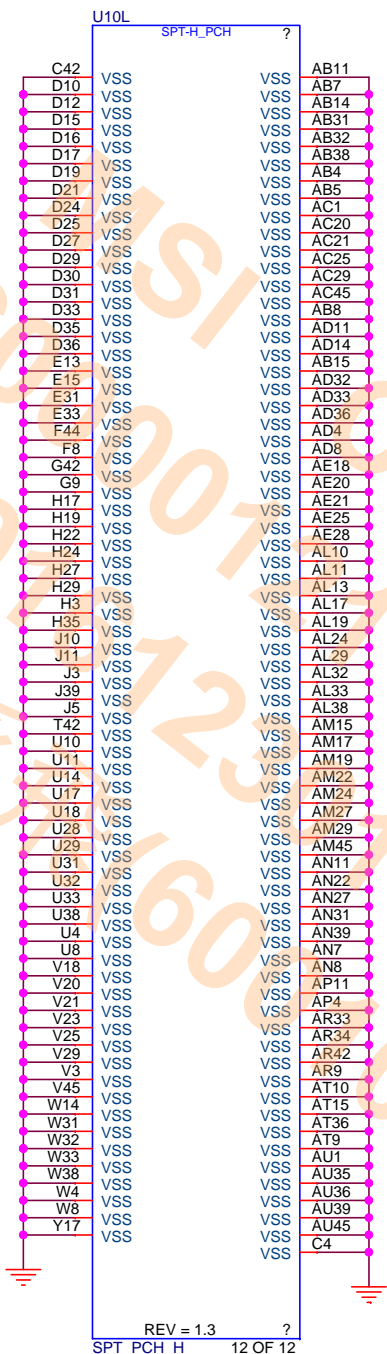
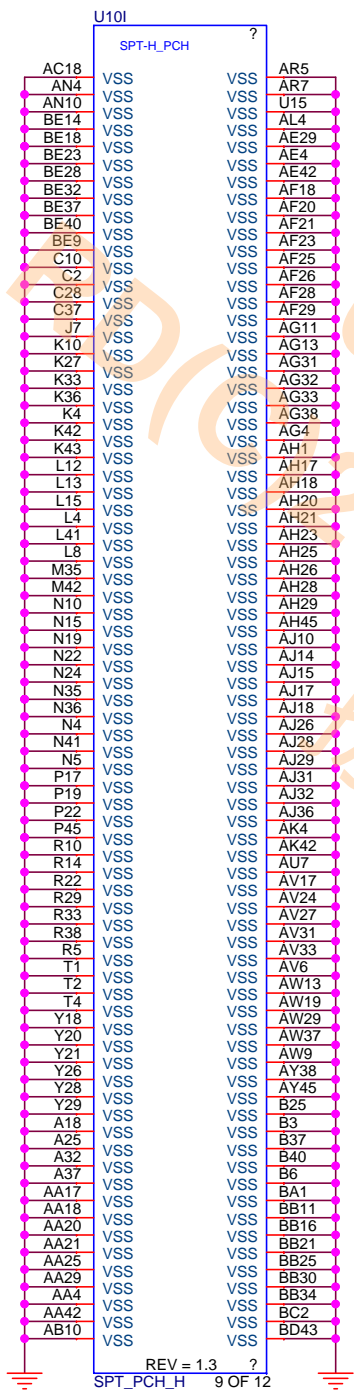
USB 2.0	USB 3.0	Device	Note
1	1	USB 3.0 Port 1	16H7A
2	2	USB 3.0 Port 2	16H7A
3			NC
4			NC
5			NC
6			NC
7		EPF021	
8			NC
9			NC
10		WLAN	
11		WebCam	
12			NC
13			NC
14			NC



High Speed I/O Ports			
Port	Device	Device	Device
1	USB3.0/PCIe	USB3.0/PCIe	WLAN
2	USB3.0/PCIe	USB3.0/PCIe	NC
3	PCIe	USB3.0/PCIe	CardReader
4	PCIe	USB3.0/PCIe	LAN
5	PCIe	PCIe	Alpine Ridge
6	PCIe	PCIe	
7	PCIe	PCIe	
8	PCIe	PCIe	
9	SATA/PCIe	SATA/PCIe	M.2 SSD 1
10	SATA/PCIe	SATA/PCIe	
11	PCIe	PCIe	
12	PCIe	PCIe	
13	PCIe	SATA/PCIe	NC
14	PCIe	SATA/PCIe	NC
15	SATA/PCIe	SATA/PCIe	NC
16	SATA/PCIe	SATA/PCIe	HDD
17	N/A	SATA/PCIe	M.2 SSD 2
18	N/A	SATA/PCIe	
19	N/A	SATA/PCIe	
20	N/A	SATA/PCIe	

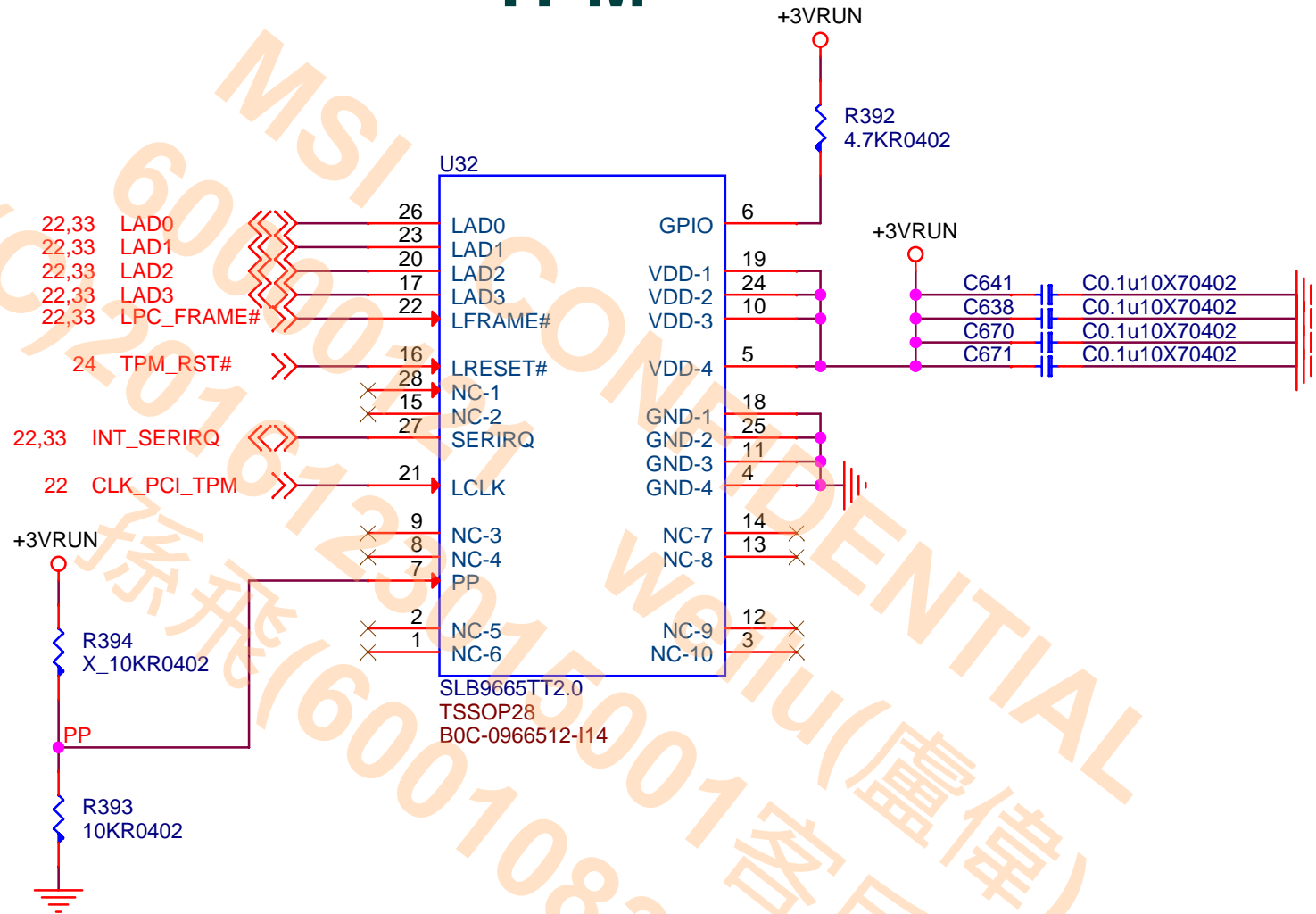






msi MICRO-STAR INT'L CO.,LTD.		
Title PCH-06 (GND)		
Size	Document Number MS-16H8	Rev 10
Date: Friday, May 22, 2015		
Sheet	26	of 63

TPM



MICRO-STAR INT'L CO.,LTD.

Title

TPM

Size

Document Number

MS-16H8

Rev

10

Date:

Friday, May 22, 2015

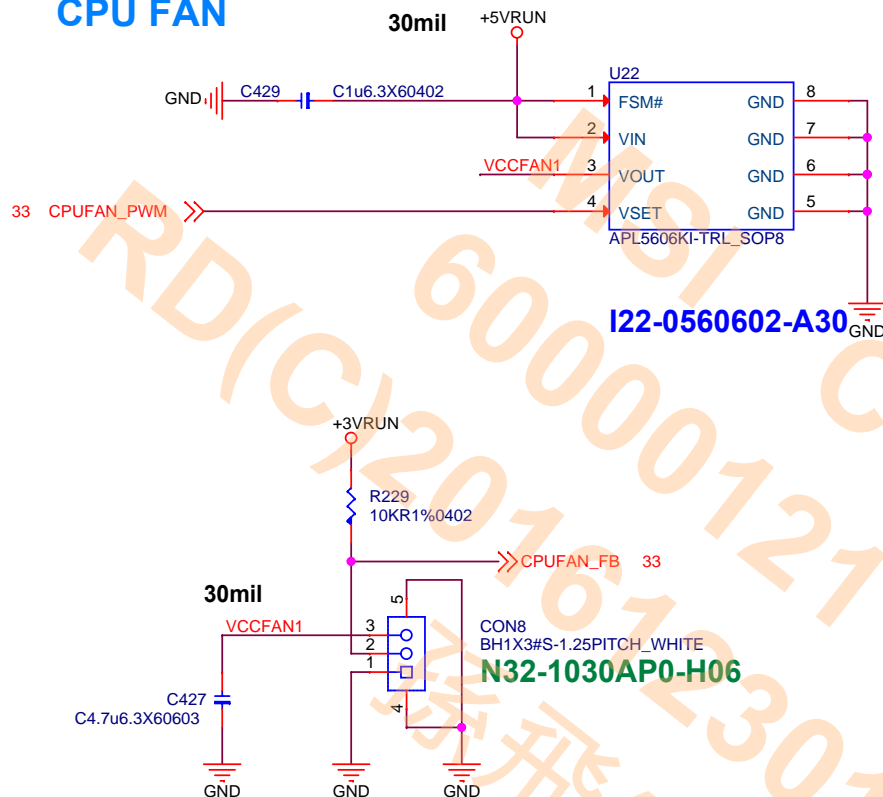
Sheet

27

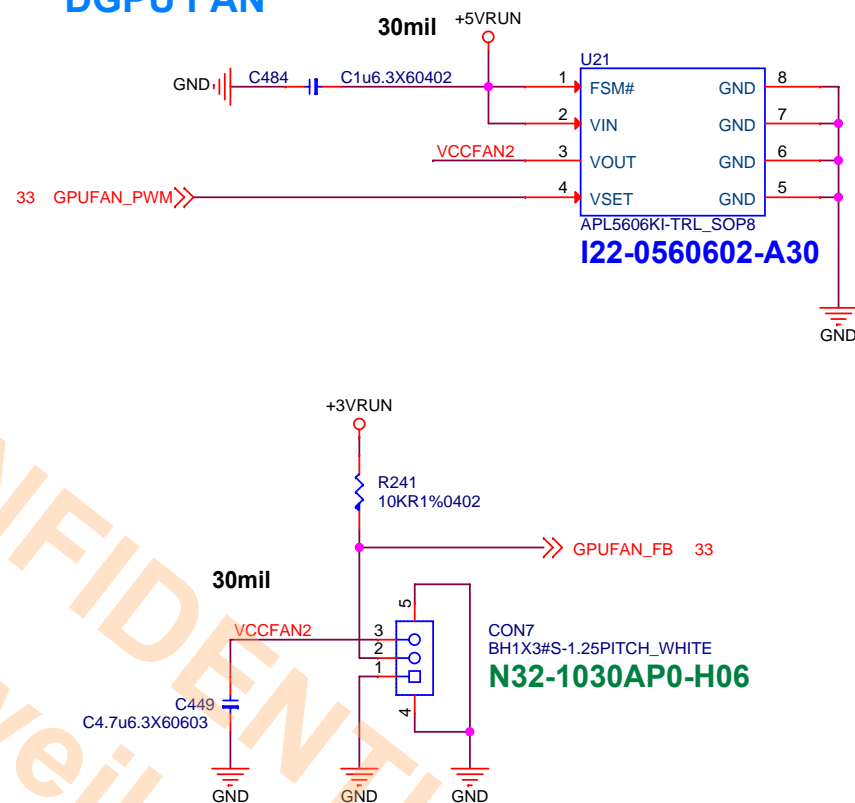
of

63

CPU FAN



DGPU FAN



MICRO-STAR INT'L CO.,LTD.

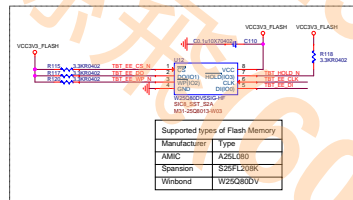
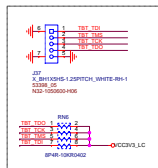
Title		
CPU FAN/DGPU FAN		
Size	Document Number	Rev
	MS-16H8	10
Date:	Sheet	
Friday, May 22, 2015	28	of 63

Thunderbolt

DDI C
HDMI

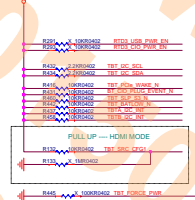
DDI B
DP

AC coupling cap. require 0201 size

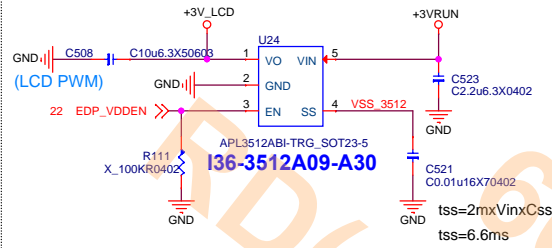


Manufacturer	Type
AMC	A2B10B0
Spanion	32SP1000
Winbond	W25Q64V

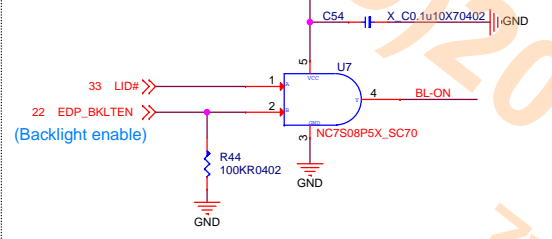
GPIO	Internal	Power Rail
GPIO_0	10K	PU
GPIO_1	10K	PU
GPIO_2	10K	PU
GPIO_3	10K	PU
GPIO_4	10K	PU
GPIO_5	10K	PU
GPIO_6	10K	PU
GPIO_7	10K	PU
GPIO_8	10K	PU
GPIO_9	10K	PU
GPIO_10	10K	PU
GPIO_11	10K	PU
GPIO_12	10K	PU
GPIO_13	10K	PU
GPIO_14	10K	PU
GPIO_15	10K	PU
GPIO_16	10K	PU
GPIO_17	10K	PU
GPIO_18	10K	PU
GPIO_19	10K	PU
GPIO_20	10K	PU
GPIO_21	10K	PU
GPIO_22	10K	PU
GPIO_23	10K	PU
GPIO_24	10K	PU
GPIO_25	10K	PU
GPIO_26	10K	PU
GPIO_27	10K	PU
GPIO_28	10K	PU
GPIO_29	10K	PU
GPIO_30	10K	PU
GPIO_31	10K	PU
GPIO_32	10K	PU
GPIO_33	10K	PU
GPIO_34	10K	PU
GPIO_35	10K	PU
GPIO_36	10K	PU
GPIO_37	10K	PU
GPIO_38	10K	PU
GPIO_39	10K	PU
GPIO_40	10K	PU
GPIO_41	10K	PU
GPIO_42	10K	PU
GPIO_43	10K	PU
GPIO_44	10K	PU
GPIO_45	10K	PU
GPIO_46	10K	PU
GPIO_47	10K	PU
GPIO_48	10K	PU
GPIO_49	10K	PU
GPIO_50	10K	PU
GPIO_51	10K	PU
GPIO_52	10K	PU
GPIO_53	10K	PU
GPIO_54	10K	PU
GPIO_55	10K	PU
GPIO_56	10K	PU
GPIO_57	10K	PU
GPIO_58	10K	PU
GPIO_59	10K	PU
GPIO_60	10K	PU
GPIO_61	10K	PU
GPIO_62	10K	PU
GPIO_63	10K	PU
GPIO_64	10K	PU
GPIO_65	10K	PU
GPIO_66	10K	PU
GPIO_67	10K	PU
GPIO_68	10K	PU
GPIO_69	10K	PU
GPIO_70	10K	PU
GPIO_71	10K	PU
GPIO_72	10K	PU
GPIO_73	10K	PU
GPIO_74	10K	PU
GPIO_75	10K	PU
GPIO_76	10K	PU
GPIO_77	10K	PU
GPIO_78	10K	PU
GPIO_79	10K	PU
GPIO_80	10K	PU
GPIO_81	10K	PU
GPIO_82	10K	PU
GPIO_83	10K	PU
GPIO_84	10K	PU
GPIO_85	10K	PU
GPIO_86	10K	PU
GPIO_87	10K	PU
GPIO_88	10K	PU
GPIO_89	10K	PU
GPIO_90	10K	PU
GPIO_91	10K	PU
GPIO_92	10K	PU
GPIO_93	10K	PU
GPIO_94	10K	PU
GPIO_95	10K	PU
GPIO_96	10K	PU
GPIO_97	10K	PU
GPIO_98	10K	PU
GPIO_99	10K	PU
GPIO_100	10K	PU



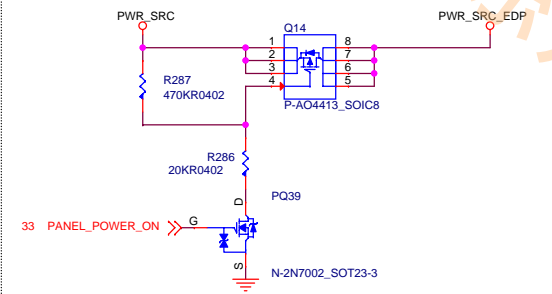
Pannel Device Logic Power



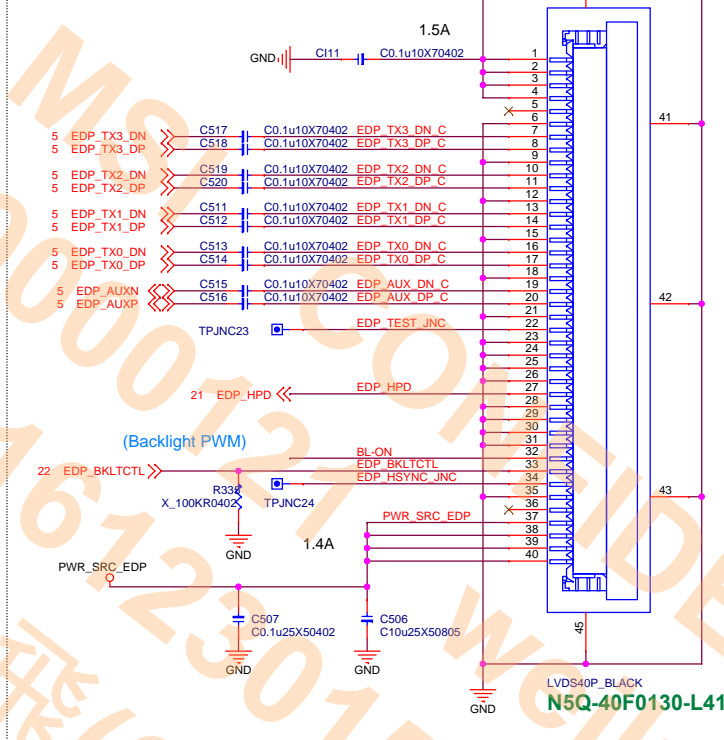
Backlight



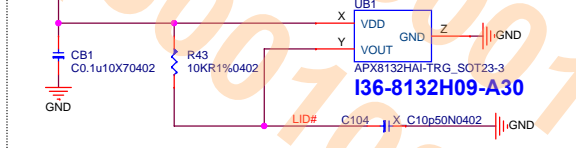
Pannel Power



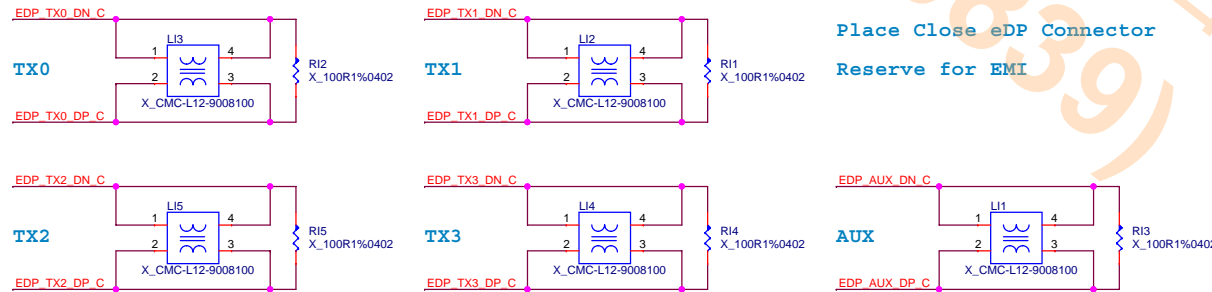
eDP CONN



Hall Switch



Place Close eDP Connector
Reserve for EMI



LCD Module Pin Define

Pin No	Symbol	Description
1	WP	EEPROM Write Protect(Keep open)
2	H_GND	High Speed Ground(0V)
3	eDP_Rx_3N	Complement Signal Link Lane 3
4	eDP_Rx_3P	True Signal Link Lane 3
5	H_GND	High Speed Ground(0V)
6	eDP_Rx_2N	Complement Signal Link Lane 2
7	eDP_Rx_2P	True Signal Link Lane 2
8	H_GND	H_GND
9	eDP_Rx_1N	Complement Signal Link Lane 1
10	eDP_Rx_1P	True Signal Link Lane 1
11	H_GND	H_GND
12	eDP_Rx_0N	Complement Signal Link Lane 0
13	eDP_Rx_0P	True Signal Link Lane 0
14	H_GND	H_GND
15	eDP_AUX_CH_P	True Signal Aux Channel
16	eDP_AUX_CH_N	Complement Signal Aux Channel
17	H_GND	H_GND
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	TEST	LCD Test Port
23	LCD_GND	LCD logic and driver ground(0V)
24	LCD_GND	LCD logic and driver ground(0V)
25	LCD_GND	LCD logic and driver ground(0V)
26	LCD_GND	LCD logic and driver ground(0V)
27	eDP_HPD	HPD signal pin
28	BL_GND	Backlight ground(0V)
29	BL_GND	Backlight ground(0V)
30	BL_GND	Backlight ground(0V)
31	BL_GND	Backlight ground(0V)
32	BL_ENABLE	Backlight enable
33	BL_PWM_DIM	System PWM signal input
34	SDA	I2C-bus Data
35	SCL	I2C-bus Clock
36	BL_PWR	Backlight power (5~21V)
37	BL_PWR	Backlight power (5~21V)
38	BL_PWR	Backlight power (5~21V)
39	BL_PWR	Backlight power (5~21V)
40	HSYNC	HSYNC output from Tcon

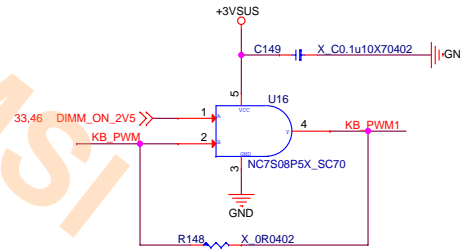
msi

MICRO-STAR INT'L CO.,LTD.

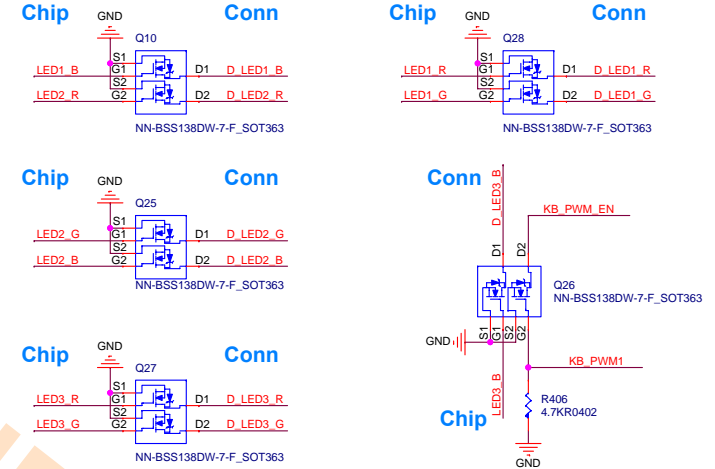
Title	eDP Connector		
Size	Document Number	Rev	10
Date:	Tuesday, May 26, 2015	Sheet	31 of 63

LED Driver IC(EPF021J)

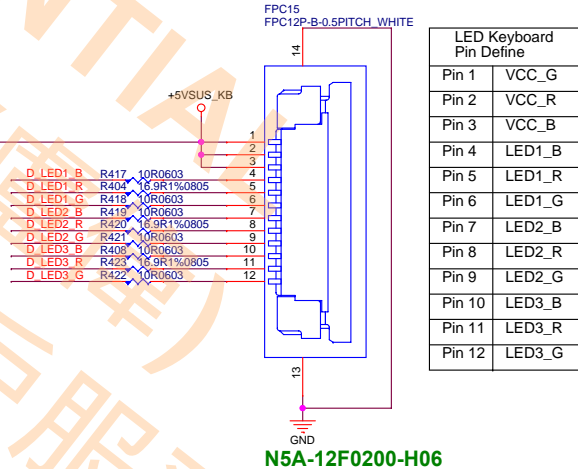
LED KB FLASH ERROR



EPF021J Sink current not enough, only using BSS138 (0.22A)



LED Keyboard CONN



LED Keyboard Pin Define	
Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G

N5A-12F0200-H06

msi MICRO-STAR INT'L CO.,LTD.	
Title LED Driver IC	
Size Document Number MS-16H8	Rev 10
Date: Friday, May 22, 2015	Sheet 32 of 63

B07-F021J14-EB3

Pin12 & Pin13 have diff branch

CardReader (RTS5249)

RTS5249 Colay RTS5227

Pin 13/15/16/22/23/24/25/26 definition are different from RTS5227

Power Trace

Pin11(3V3_IN) / Pin 12(CARD_3V3)trace fixed width is 40 mils (minimum)

Pin27(3V3aux) / Pin 13(SD_VDD2)trace fixed width is 30 mils (minimum)

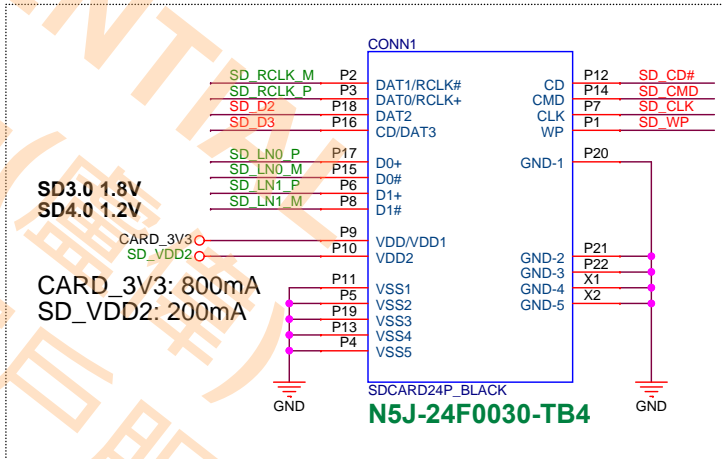
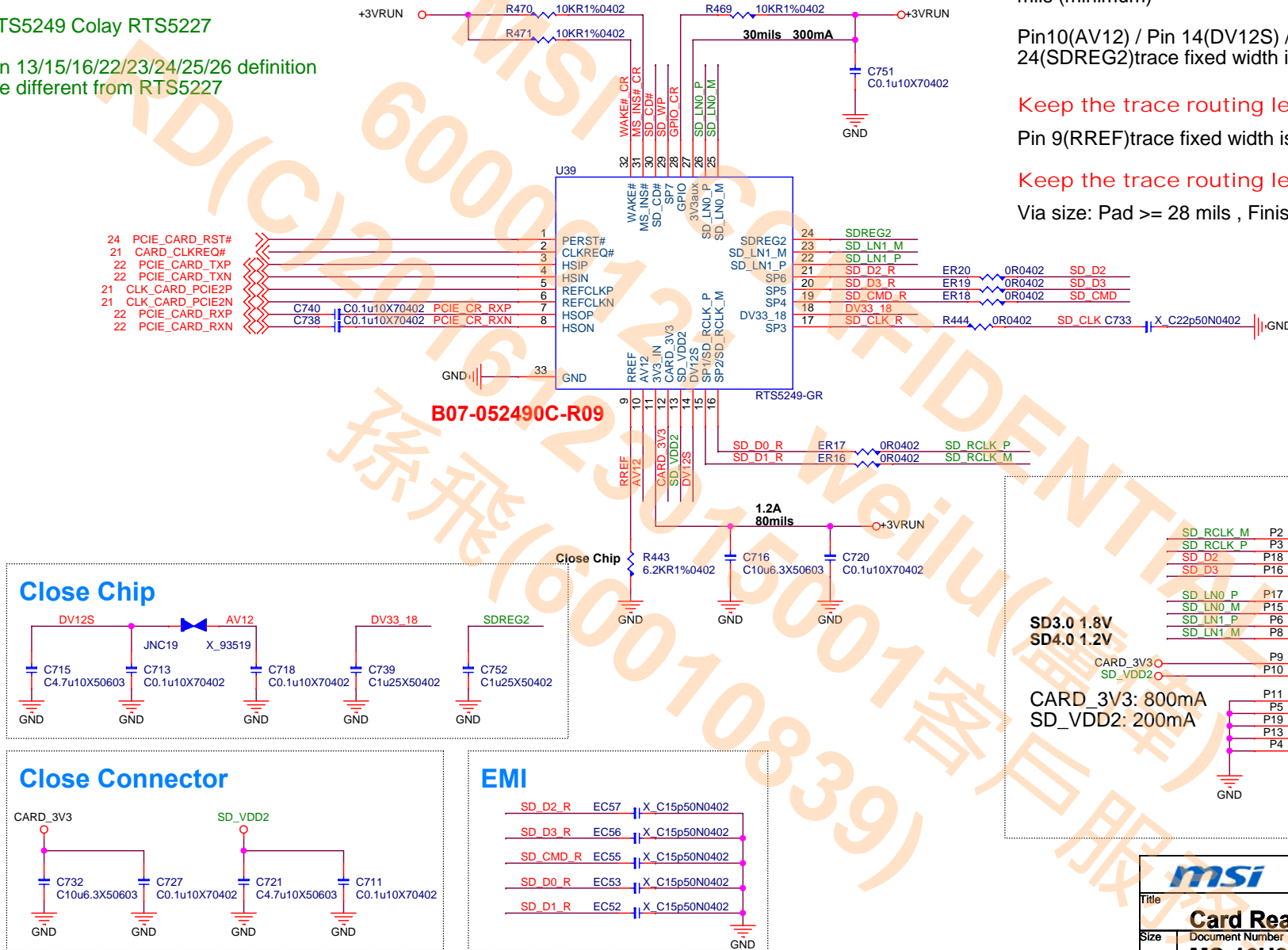
Pin10(AV12) / Pin 14(DV12S) / Pin 18(DV33_18) / Pin 24(SDREG2)trace fixed width is 20 mils (minimum)

Keep the trace routing lengths is limit to 200 mils

Pin 9(RREF)trace fixed width is 12 mils (minimum)

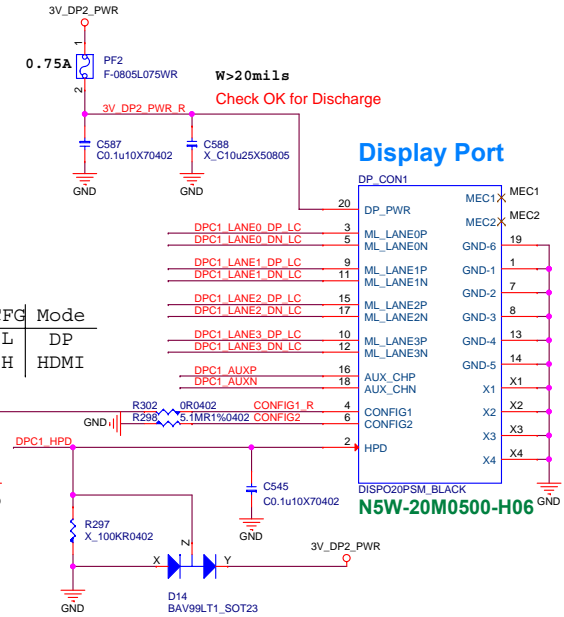
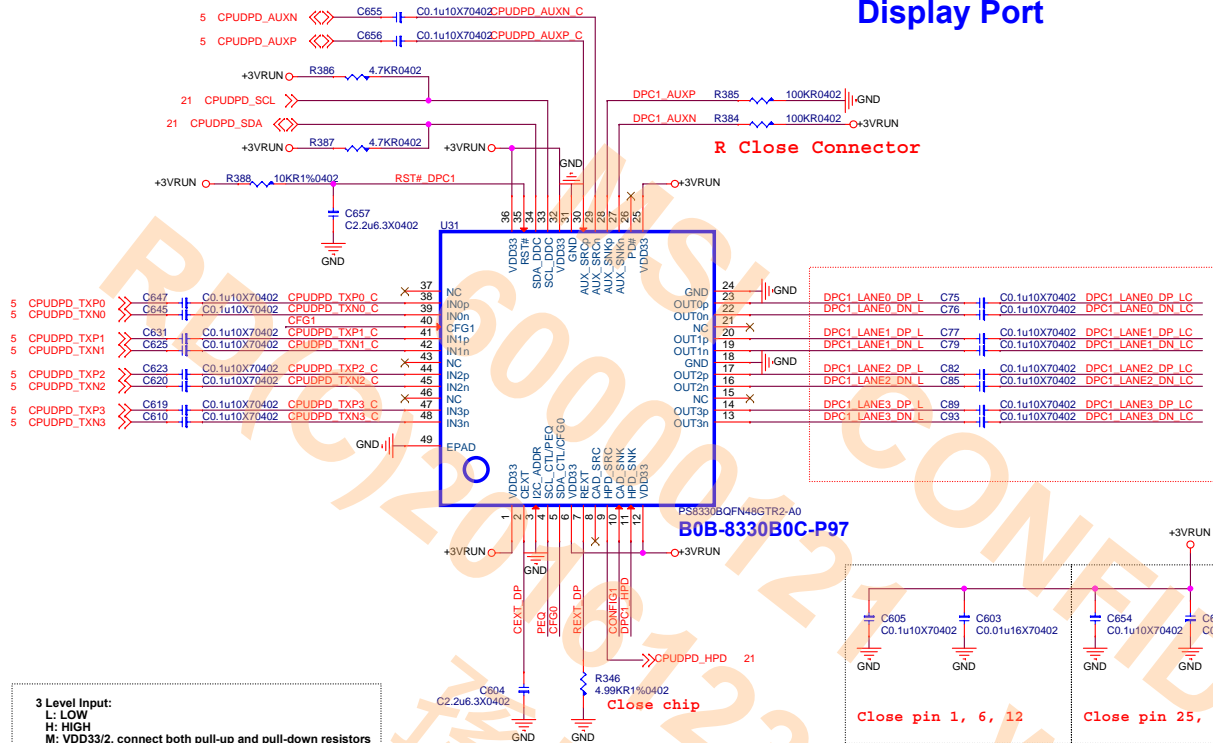
Keep the trace routing lengths is limit to 200 mils

Via size: Pad >= 28 mils , Finished hole >= 16 mils.

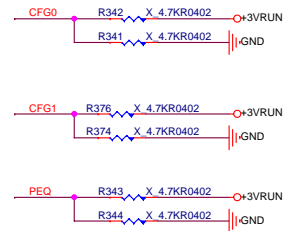


Title		Card Reader	
Size	Document Number	MS-16H8	
Date:	Friday, May 22, 2015	Sheet	34 of 63
Rev		10	

Display Port



CAD_SNK Have internal Pull down 1Mohm.
HPD_SNK Have internal Pull down 150kohm.
No problem with Leakage from DP device
The DP_PWR and RETURN pins of the box-to-box connectors must support the maximum current rating of 500mA.

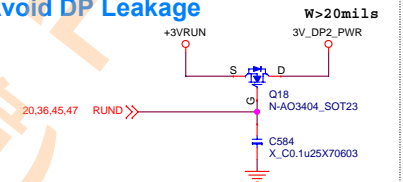


Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150k Ohm, 3.3V I/O.
L: default, automatic EQ enable & AUX interception enable
H: automatic EQ disable & AUX interception enable
M: automatic EQ disable & AUX interception disable, no pre-emphasis, 600mVpp swing

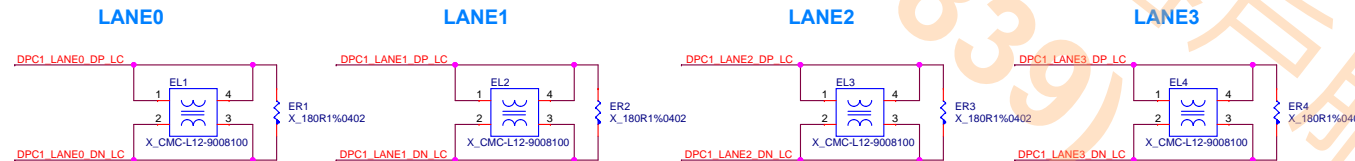
Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at ~150K Ohm
H: default, auto test disable & input offset cancellation enable
L: auto test enable & input offset cancellation enable
M: auto test disable & input offset cancellation disable

Programmable input equalization levels; Internal pull down at ~150K Ohm, 3.3V I/O.
L: default, LBQ, compensate channel loss up to 12dB @ HBR2
H: HBQ, compensate channel loss up to 15dB @ HBR2
M: LLBQ, compensate channel loss up to 5dB @ HBR2

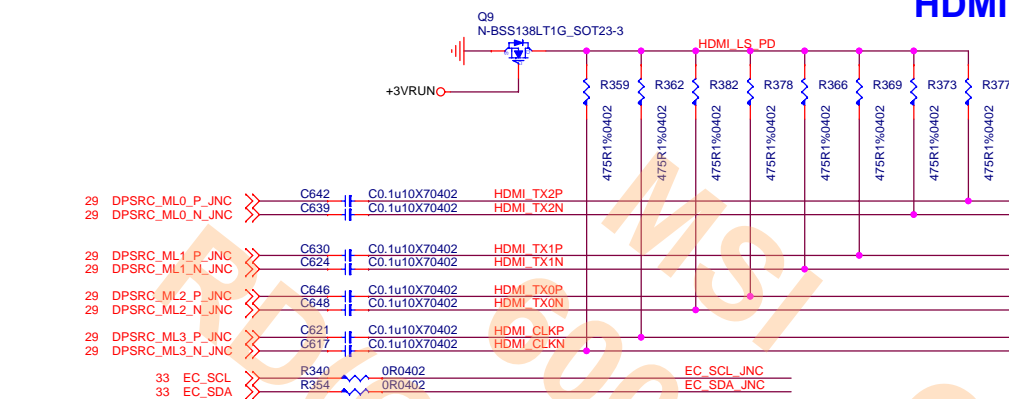
Avoid DP Leakage



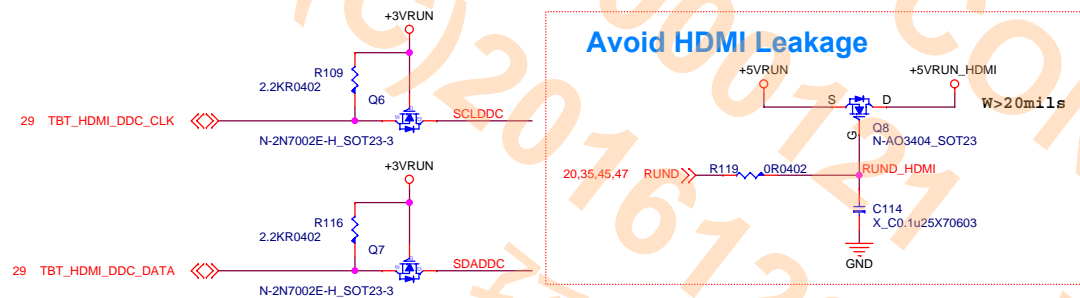
EMI Close Connector



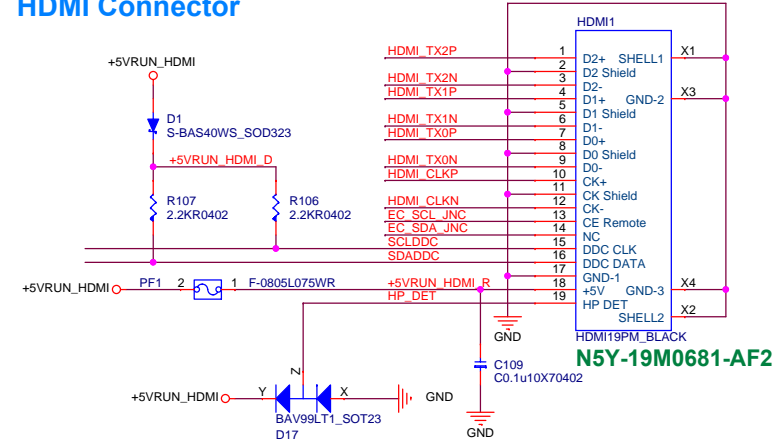
HDMI Repeater



Avoid HDMI Leakage

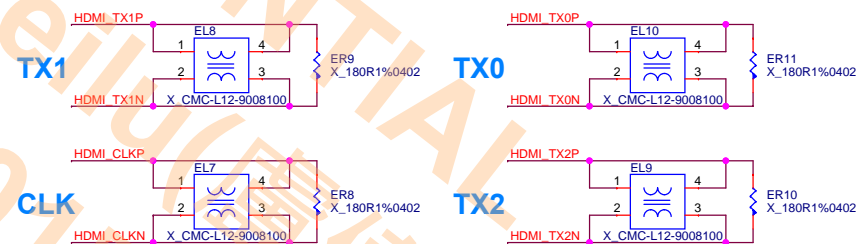


HDMI Connector



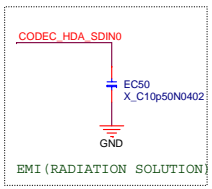
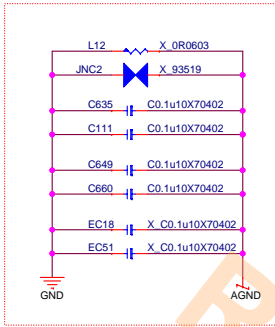
An HDMI Source shall have +5V Power signal over-current protection of no more than 0.5A.

EMI Close Connector

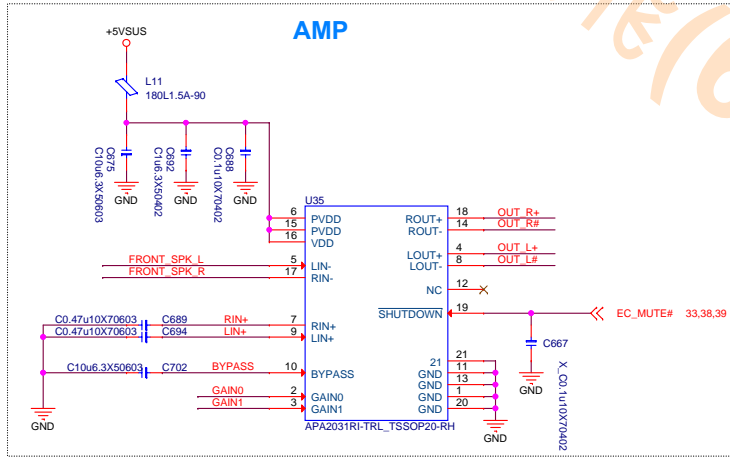
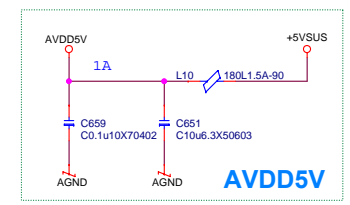
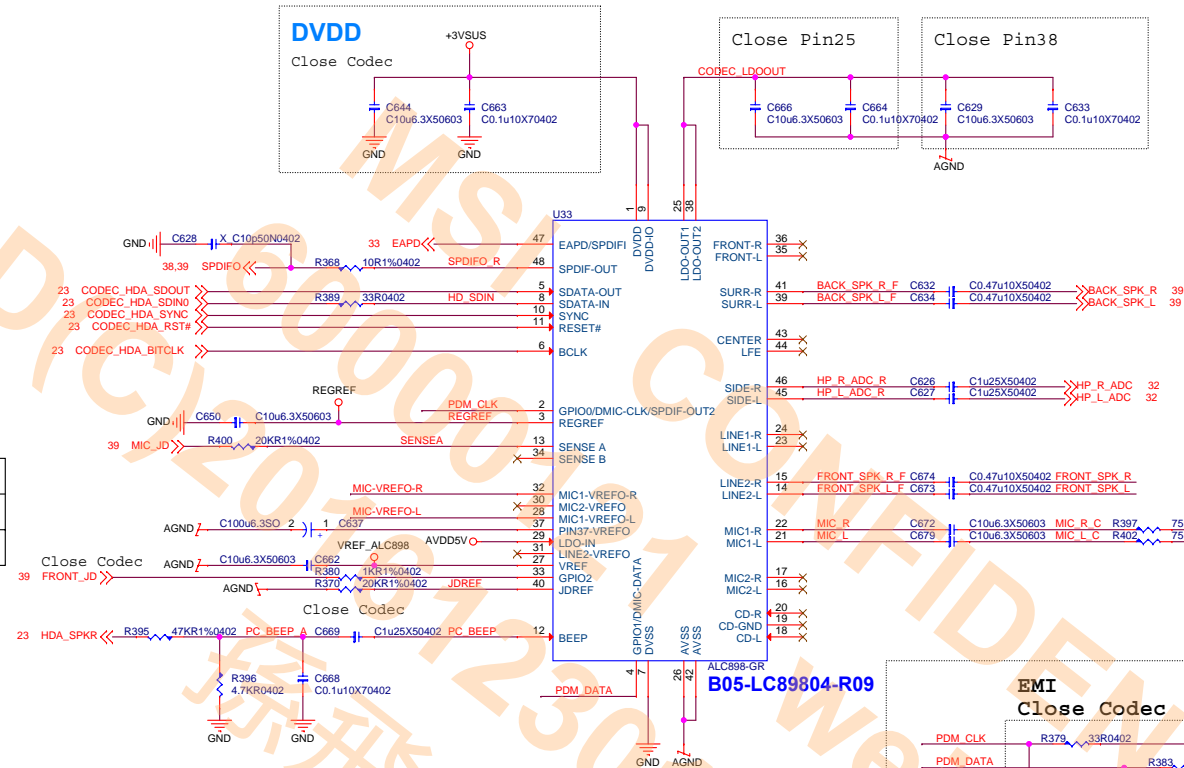


msi MICRO-STAR INT'L CO.,LTD.		
Title		
HDMI Repeater		
Size	Document Number	Rev
MS-16H8		10
Date:	Friday, May 22, 2015	Sheet 36 of 63

Audio CODEC(ALC898/ALC892)/Audio AMP(APA2031)

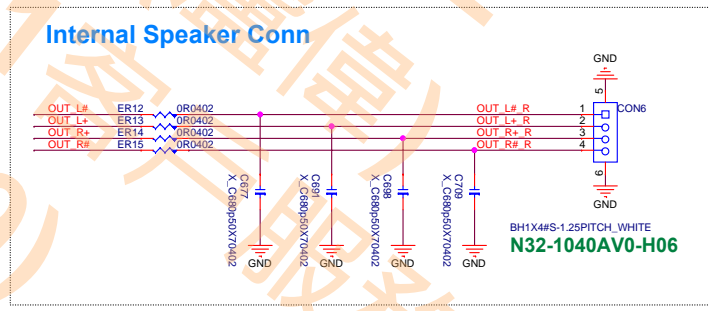
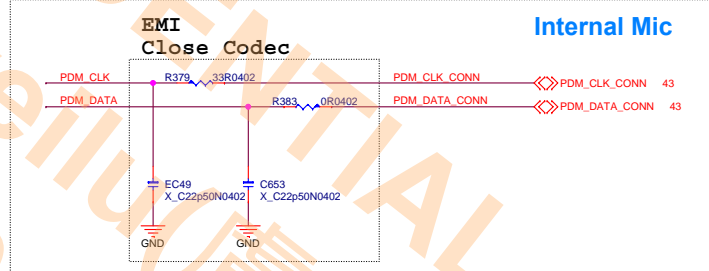
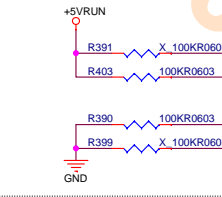


PIN 37 - VREFO	
ALC892	NC
ALC898	Stuff

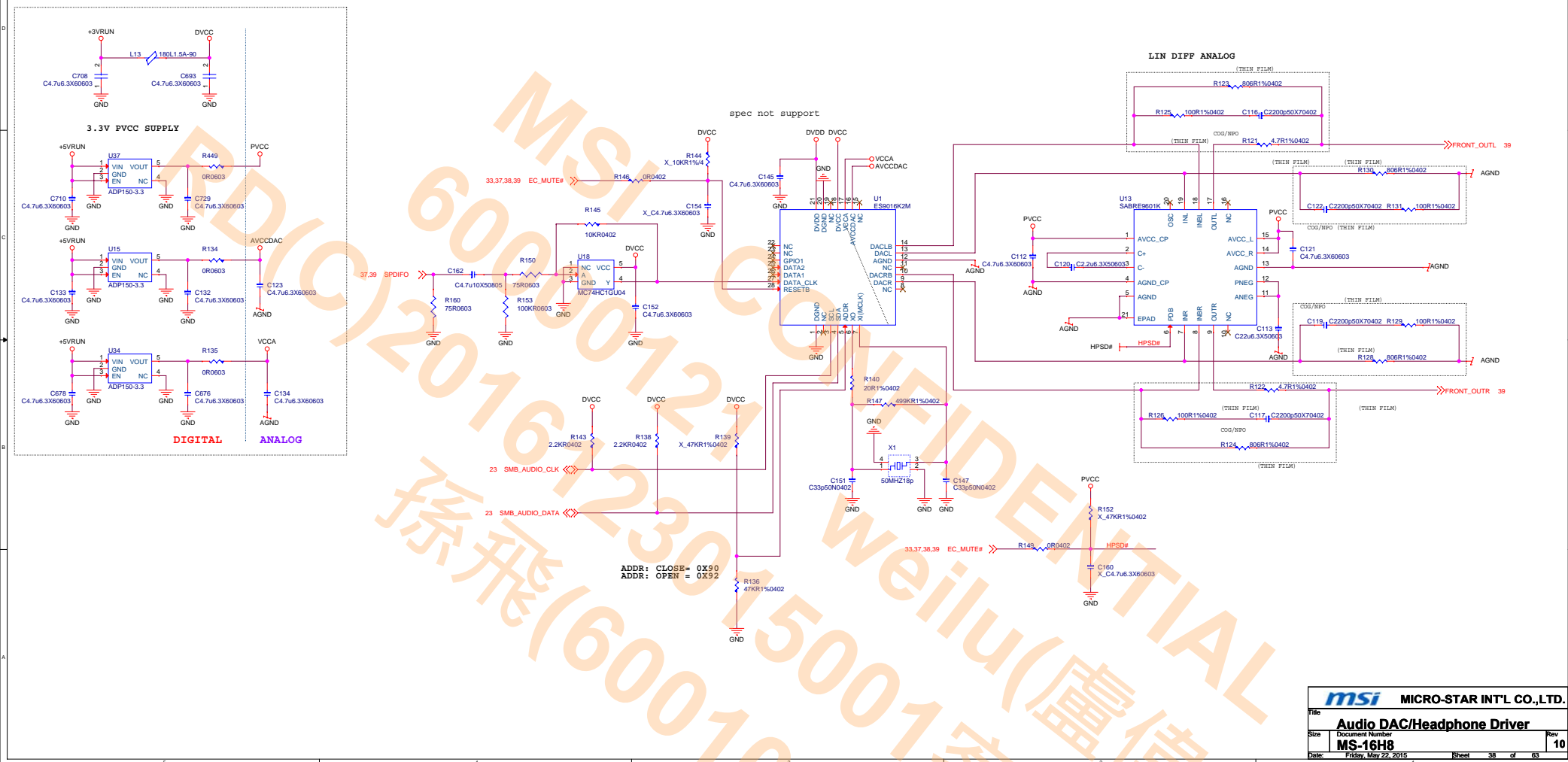


For APA2031

Av	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1
4.3dB	X	X

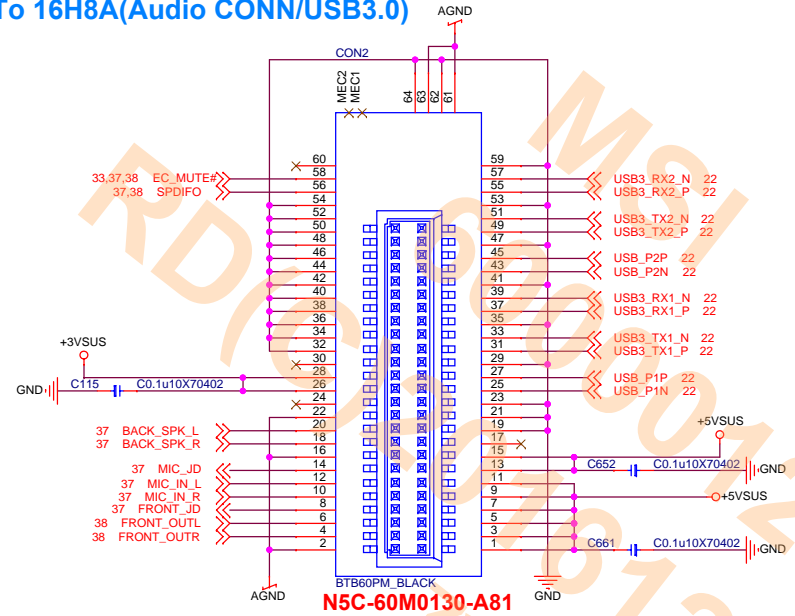


Audio DAC(ES9018)/Headphone Driver(SABRE9601)

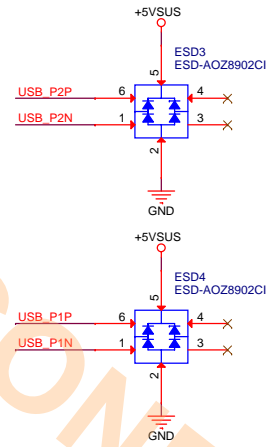


BTB CONN

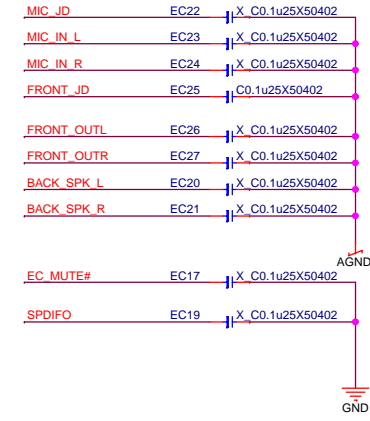
To 16H8A(Audio CONN/USB3.0)



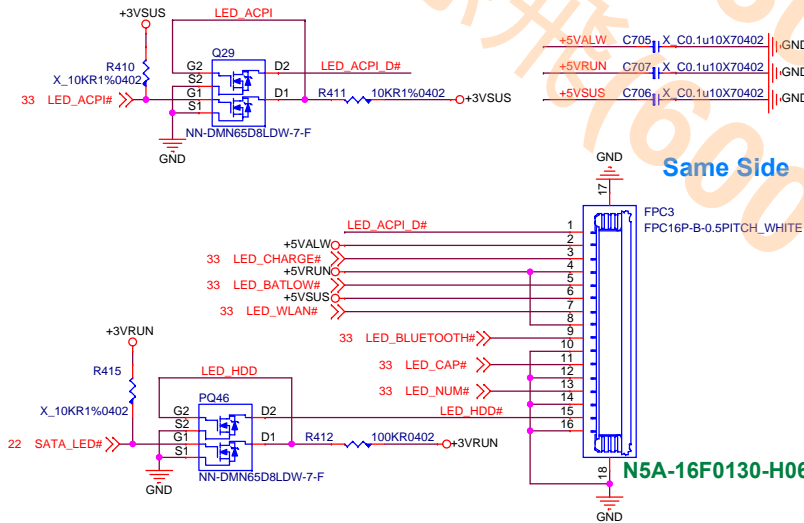
ESD



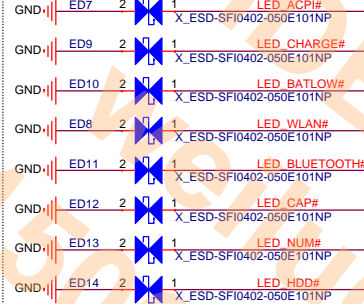
EMI



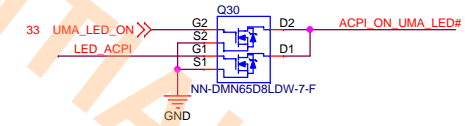
To 16H8B(LED Board)



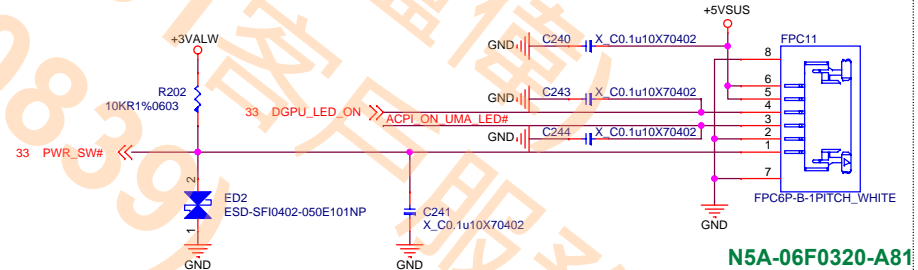
EMI



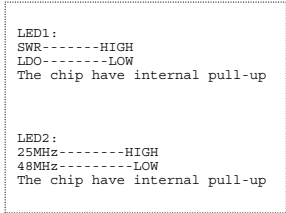
S3 Breath S0 No active



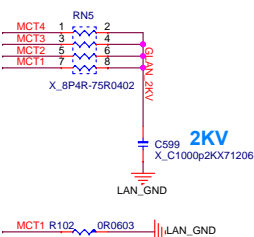
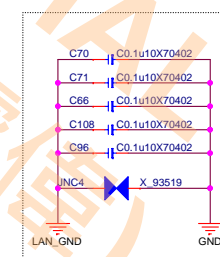
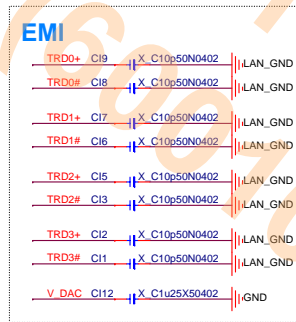
To 16H8C (Power Board)



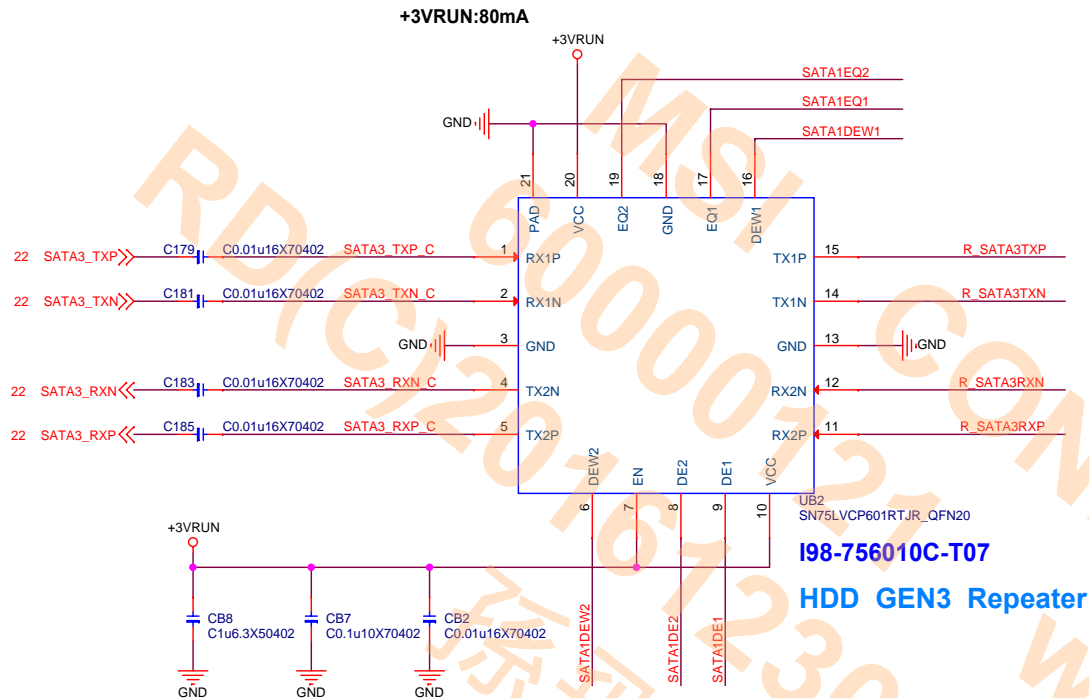
GIGA LAN(BFN2400/AR8161)



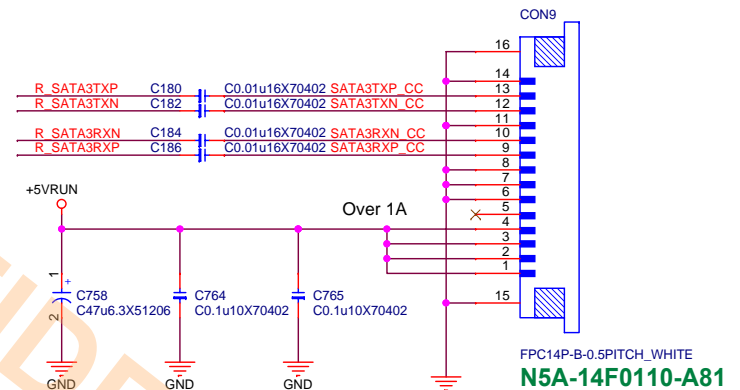
PIN 38 (LAN_LED0)	
AR8161	NC
E2400	Stuff



HDD (With Repeater)



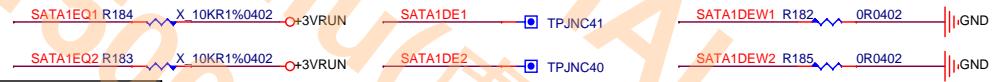
BTB Connector



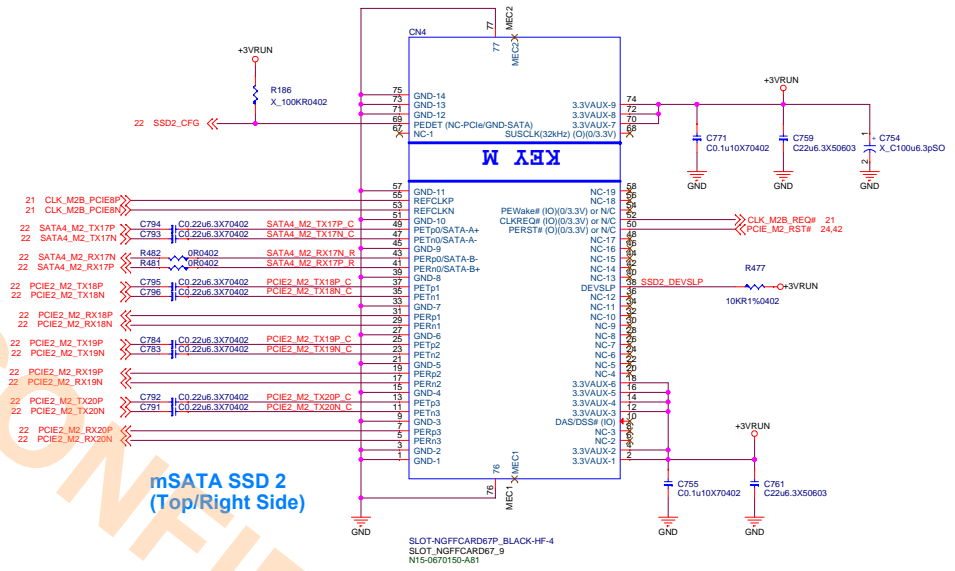
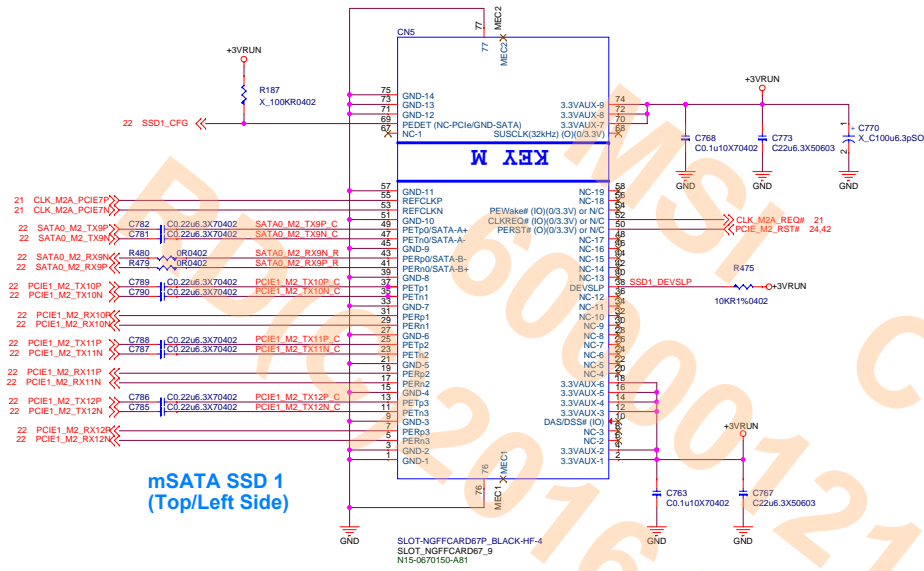
TI SN75LVCP601RTJR HW Setting

DE1/DE2	CH1/CH2De-Emphasis dB (at 6Gbps)	DQ1/DQ2	CH1/CH2De-Emphasis dB (at 6Gbps)
NC (default)	-4	NC (default)	0
0	0	0	7
1	-2	1	14

DEW1/DEW2	Device Function --> De Width for CH1/CH2
0	De-emphasis Pulse duration, short (recommended setting when link operates at SATA 1.5/3/6 Gbps)
1 (default)	De-emphasis Pulse duration, long (recommended setting when link operates at SATA 1.5/3/6 Gbps)

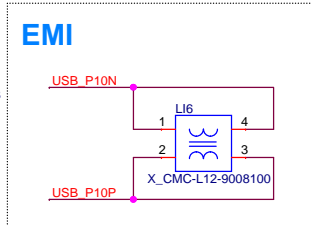
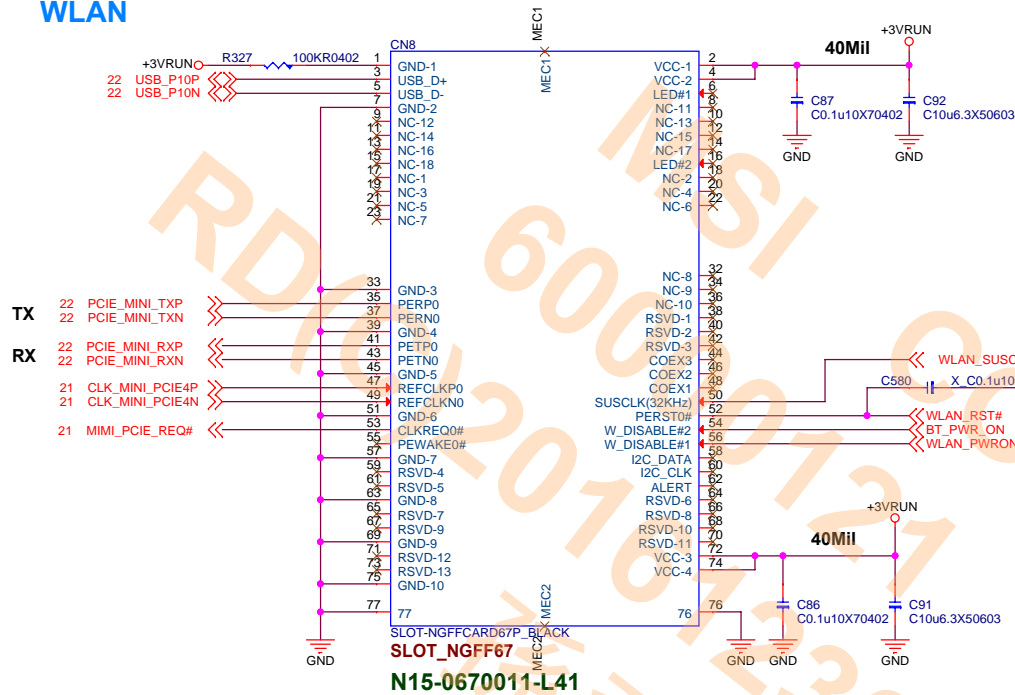


SSD



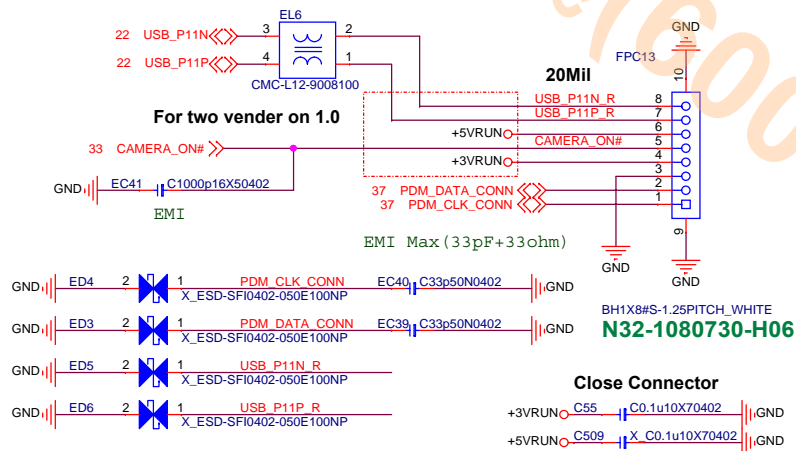
msi MICRO-STAR INT'L CO.,LTD.		
File		
SSD		
Size	Document Number	Rev
	MS-16H8	10
Date	Monday, May 25, 2015	Sheet 42 of 63

WLAN

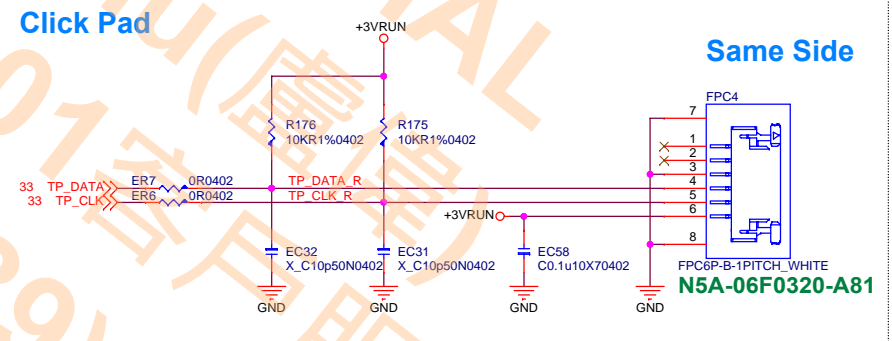


Pin 1	GND	Pin 2	3.3V
Pin 3	USB_D+	Pin 4	3.3V
Pin 5	USB_D-	Pin 6	LED1#
Pin 7	GND	Pin 8	Module Key
Pin 9	Module Key	Pin 10	Module Key
Pin 11	Module Key	Pin 12	Module Key
Pin 13	Module Key	Pin 14	Module Key
Pin 15	Module Key	Pin 16	LED2#
Pin 17	N/C	Pin 18	GND
Pin 19	N/C	Pin 20	N/C
Pin 21	N/C	Pin 22	N/C
Pin 23	N/C	Pin 24	Module Key
Pin 25	Module Key	Pin 26	Module Key
Pin 27	Module Key	Pin 28	Module Key
Pin 29	Module Key	Pin 30	Module Key
Pin 31	Module Key	Pin 32	N/C
Pin 33	GND	Pin 34	N/C
Pin 35	PERP0	Pin 36	N/C
Pin 37	PERN0	Pin 38	Clink Reset (I 3.3V)
Pin 39	GND	Pin 40	N/C
Pin 41	PETP0	Pin 42	N/C
Pin 43	PETN0	Pin 44	N/C
Pin 45	GND	Pin 46	N/C
Pin 47	REFCLKP0	Pin 48	N/C
Pin 49	REFCLKN0	Pin 50	N/C (SUSCLK (32kHz) for DSx)
Pin 51	GND	Pin 52	PERST0#
Pin 53	CLKREQ0#	Pin 54	BT_EN (W_DISABLE2#)
Pin 55	PEWAKE0#	Pin 56	WLAN_EN (W_DISABLE2#)
Pin 57	GND	Pin 58	N/C
Pin 59	N/C	Pin 60	N/C
Pin 61	N/C	Pin 62	N/C
Pin 63	GND	Pin 64	Resever
Pin 65	N/C	Pin 66	N/C
Pin 67	N/C	Pin 68	N/C
Pin 69	GND	Pin 70	N/C
Pin 71	N/C	Pin 72	3.3V
Pin 73	N/C	Pin 74	3.3V
Pin 75	GND		

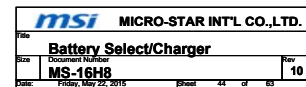
CAMERA



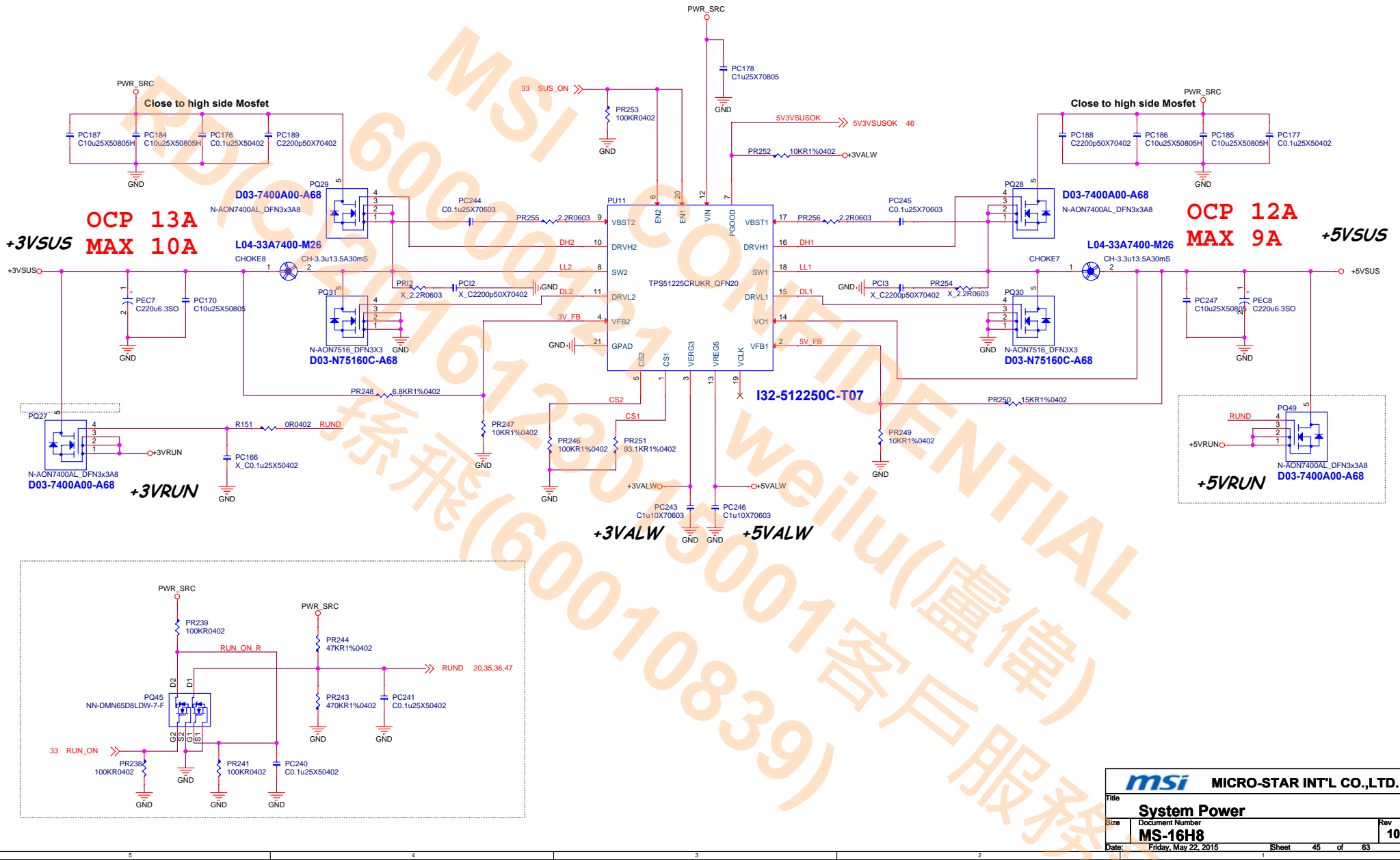
Click Pad



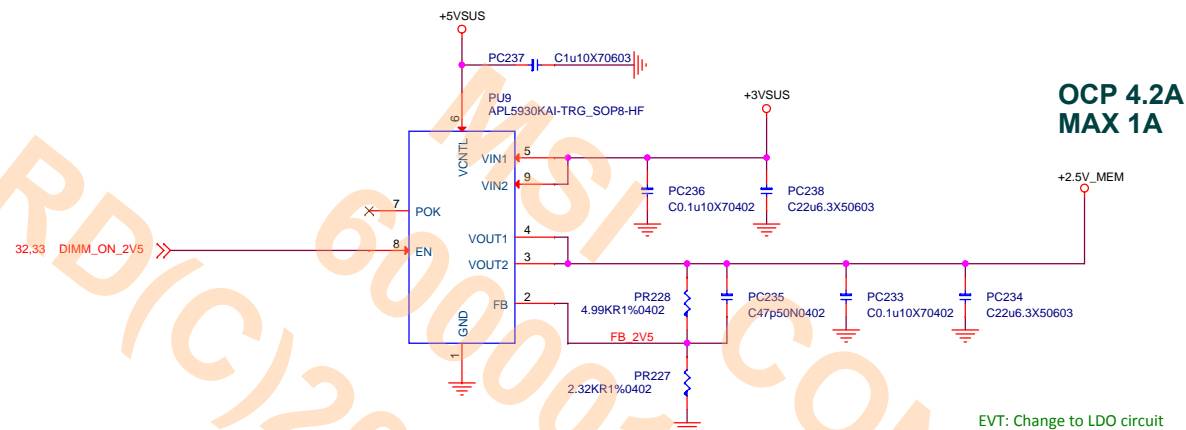
Battery Select



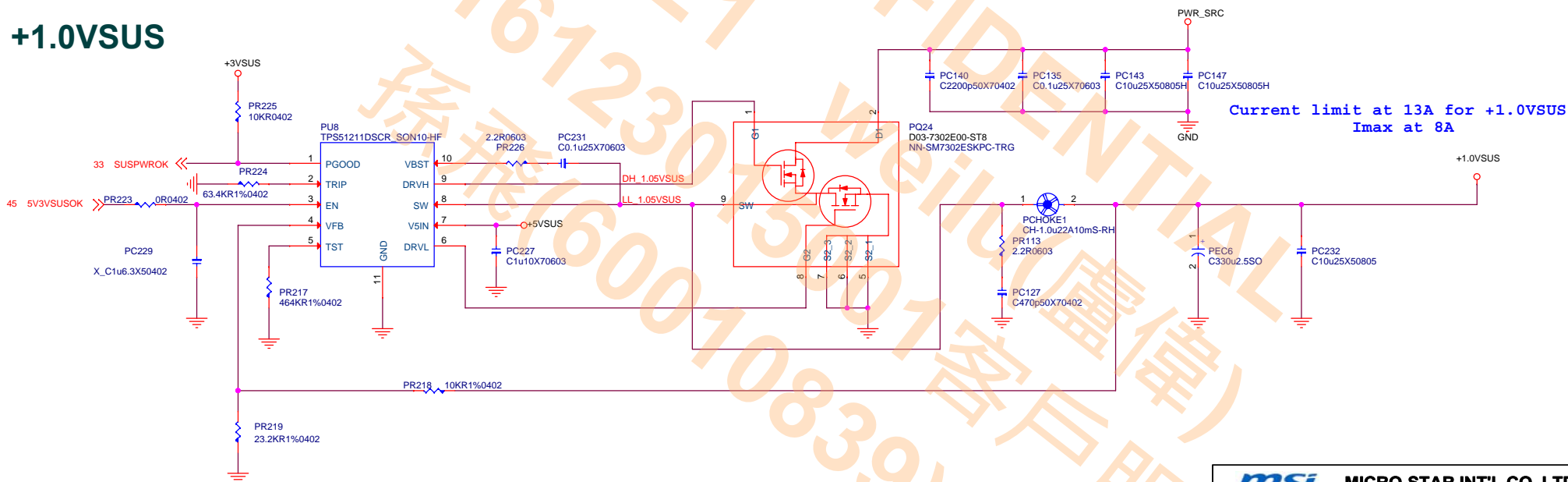
System Power




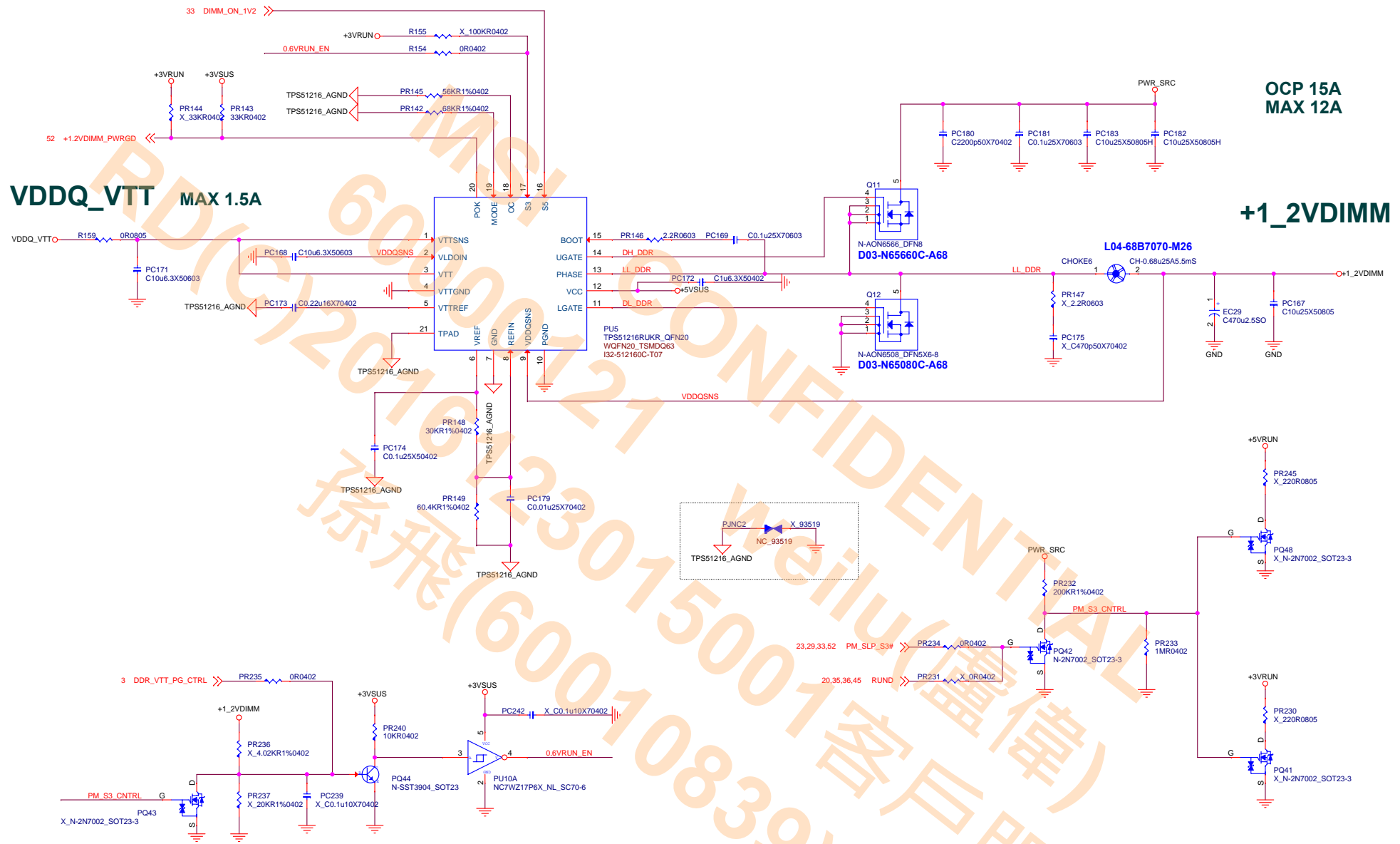
+2.5V_MEM



+1.0VSUS



		MICRO-STAR INT'L CO.,LTD.	
Title			
2.5VMEM/1.0VSUS			
Size	Document Number		Rev
MS-16H8		10	
Date:	Tuesday, May 26, 2015	Sheet	46 of 63



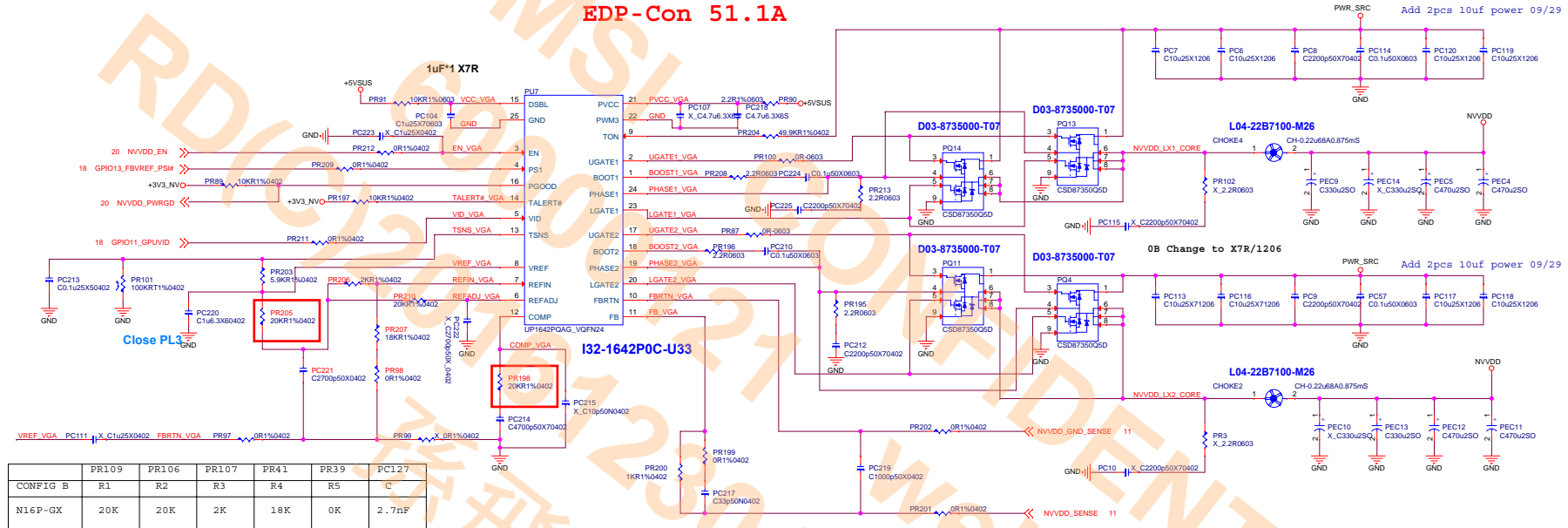
DGPU POWER NVVDD

CONFIG B
VBoot:0.9V
Vmin:0.6V / Vmax:1.2V

EDP-Peak 87A
EDP-Con 51.1A

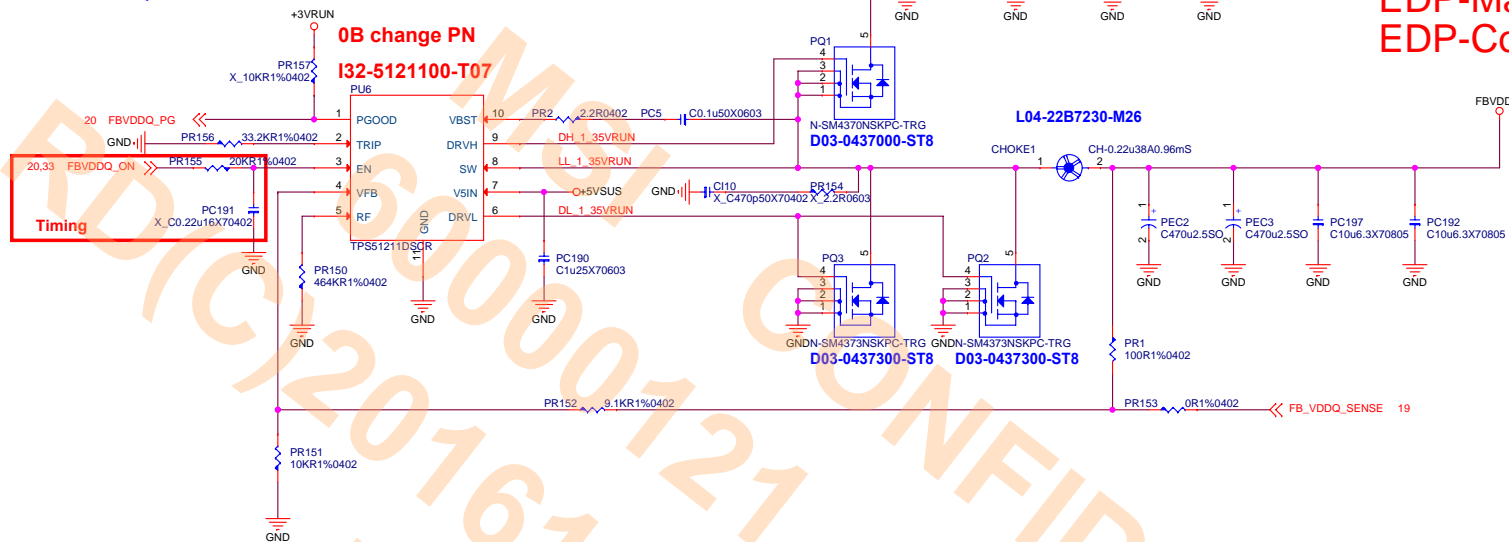
0B Change to X7R/1206
1.0 Change to X5R/1206 high

PWR_SRC Add 2pcs 10uf power 09/29



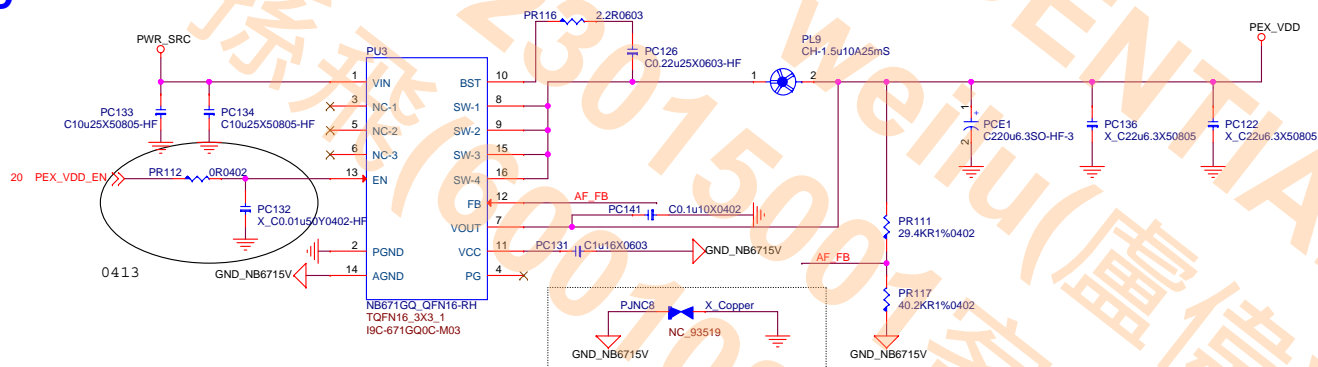
	PR109	PR106	PR107	PR41	PR39	PC127
CONFIG B	R1	R2	R3	R4	R5	C
N16P-GX	20K	20K	2K	18K	0K	2.7nF

FBVDDQ



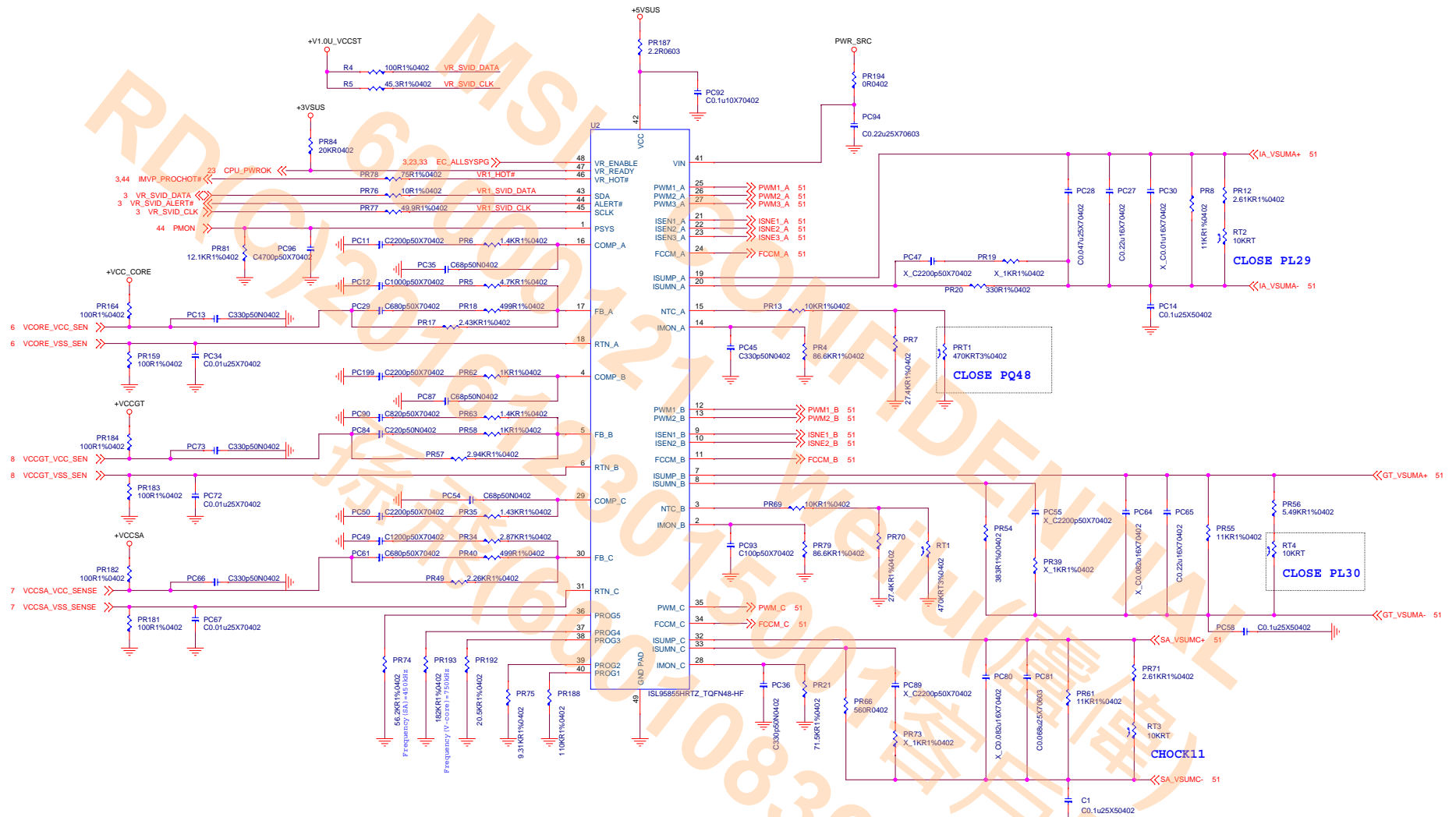
OCP 30A
EDP-Max 25
EDP-Con 17A

PEX_VDD



OCP 8A
MAX 6A

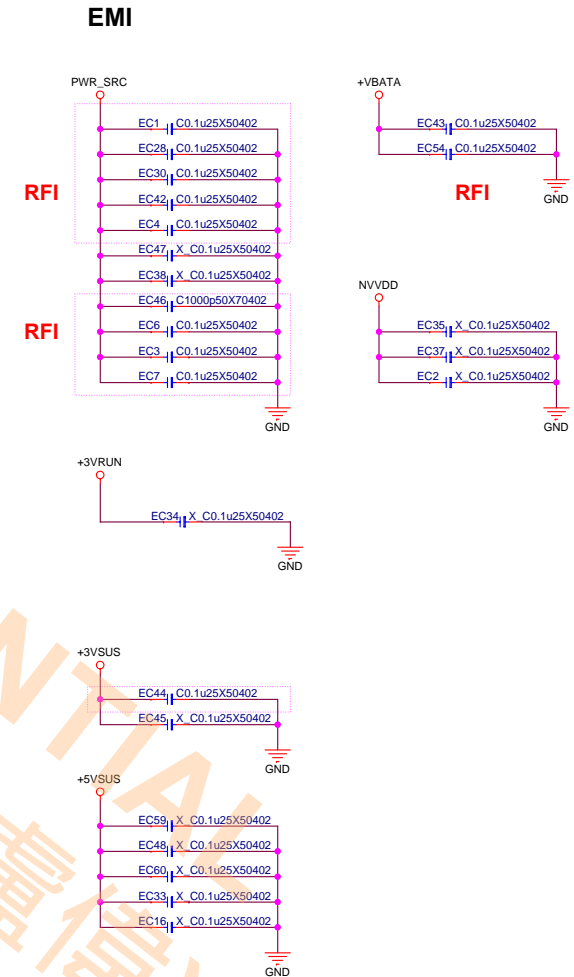
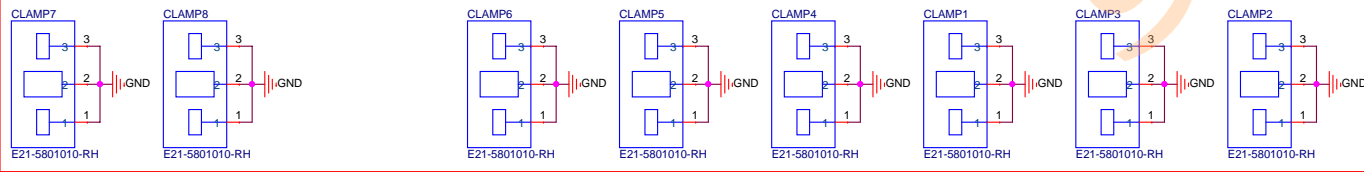
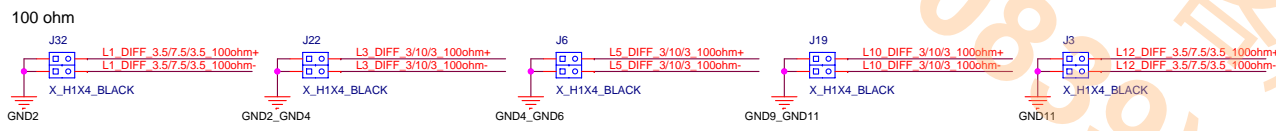
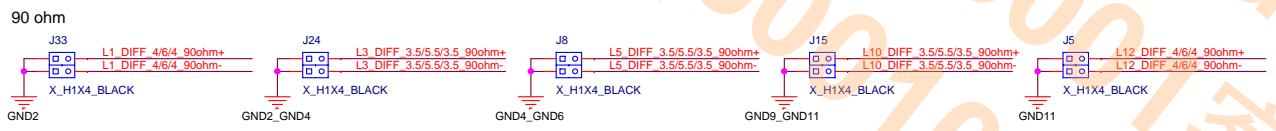
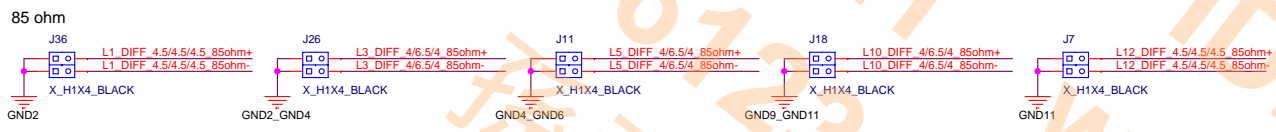
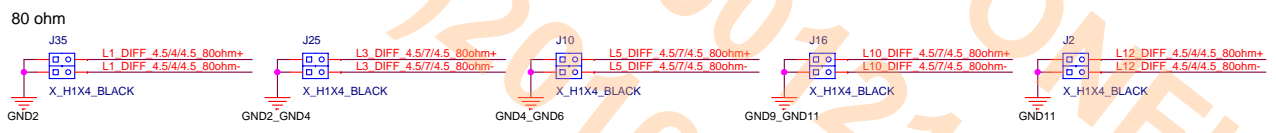
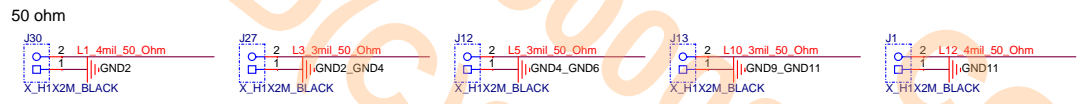
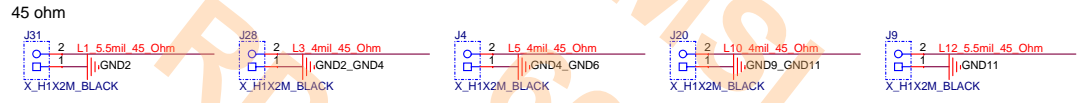
CPU Power IC (ISL95855)



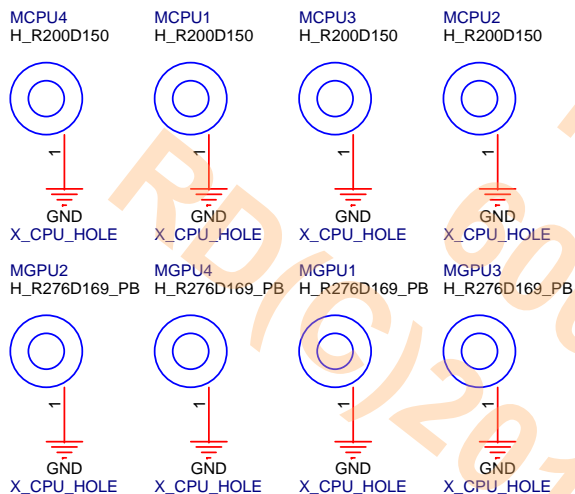


EMI/ Impedance

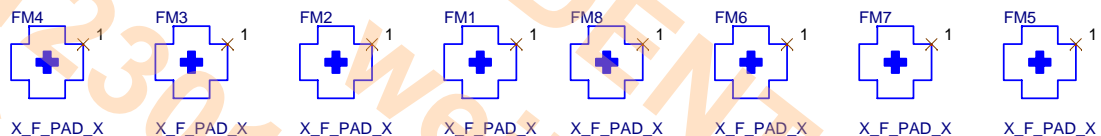
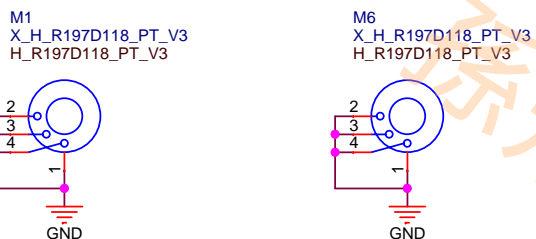
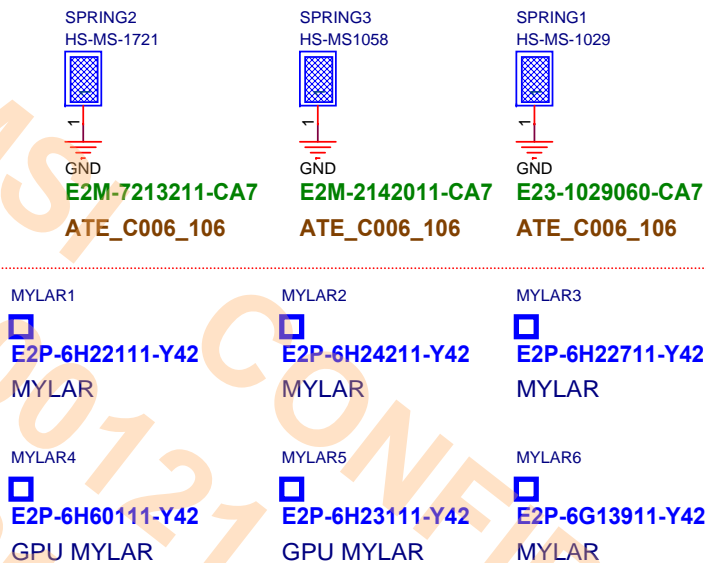
Impedance Connector No PN



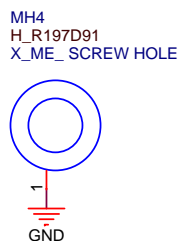
CPU/GPU Holes



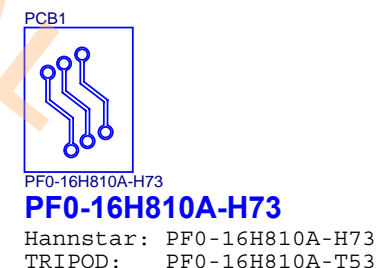
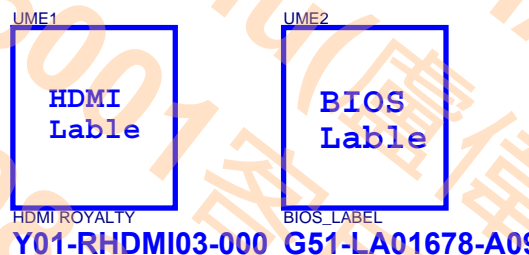
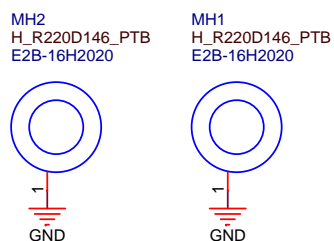
EMI



Fan Hole



SSD Stand off



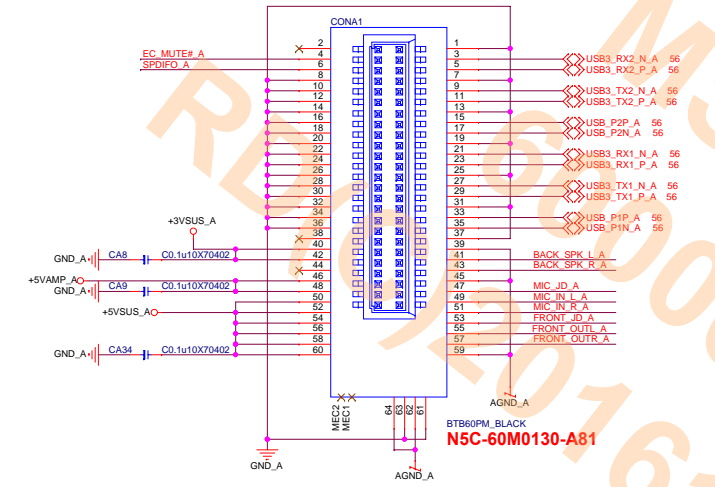
msi

MICRO-STAR INT'L CO.,LTD.

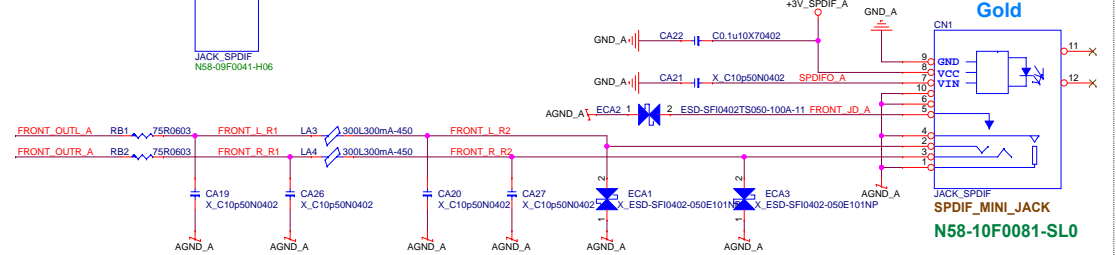
Title		
Screw/ME		
Size	Document Number	Rev
	MS-16H8	10
Date:	Tuesday, May 26, 2015	Sheet 54 of 63

16H8A Board (Audio CONN)

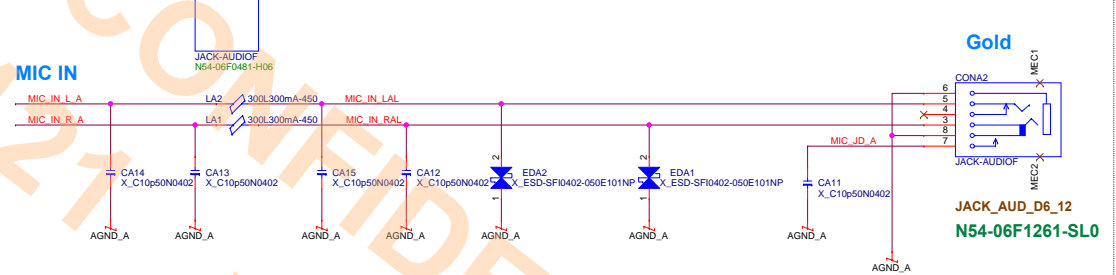
BTB Connector From MB CONN Pin Current Capability : 0.5A/Pin



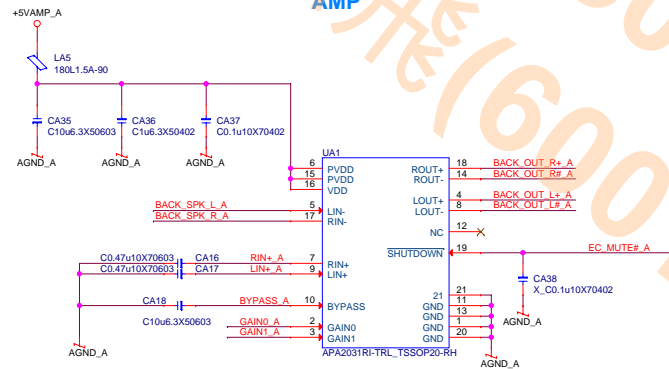
FRONT OUT



MIC IN

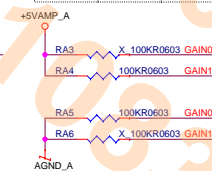


AMP

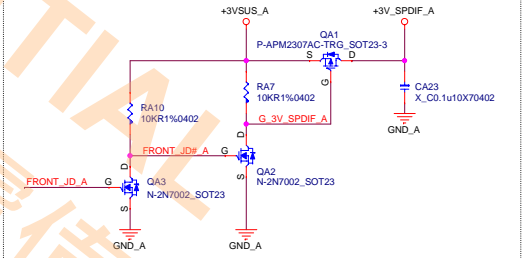


For APA2031

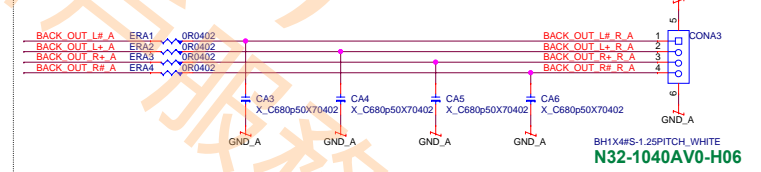
Av	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1
4.3dB	X	X



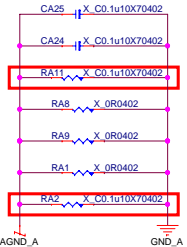
SPDIF Power



BACK SPK CONN



EMI

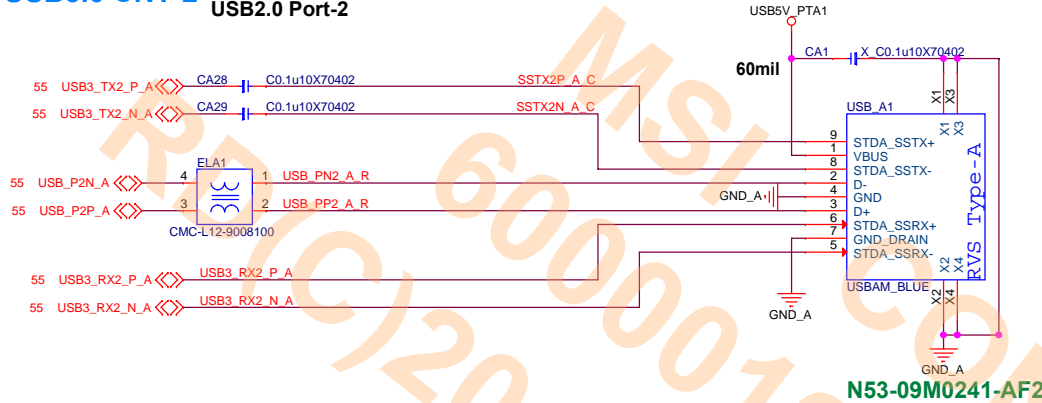


Change to Cap

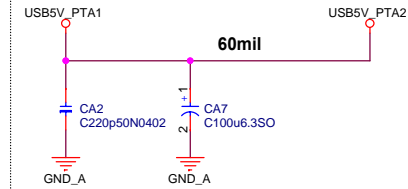
Change to Cap

16H8C USB3.0 CNT-2/3

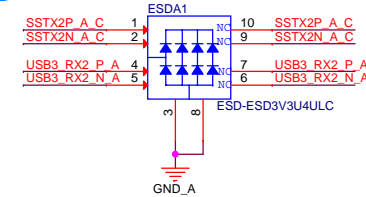
USB3.0 CNT-2 USB3.0 Port-2 USB2.0 Port-2



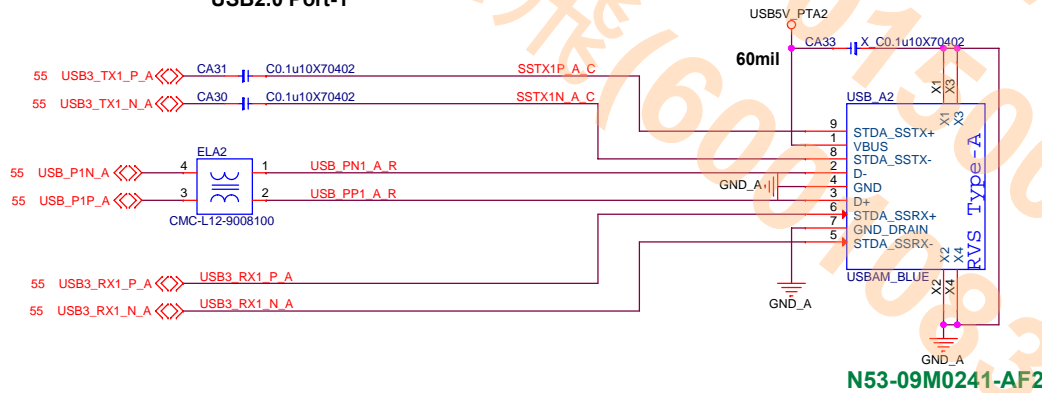
USB Power



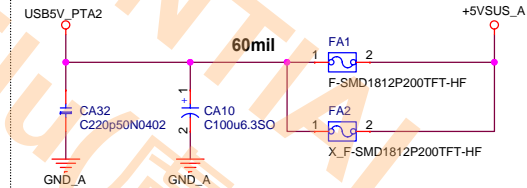
ESD



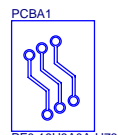
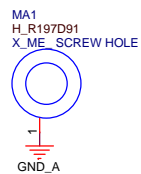
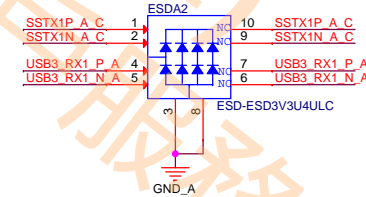
USB3.0 CNT-3 USB3.0 Port-1 USB2.0 Port-1



USB Power



ESD



PF0-16H8A0A-H73
PF0-16H8A0A-H73

Hannstar: PF0-16H8A0A-H73
TRIPOD: PF0-16H8A0A-T53

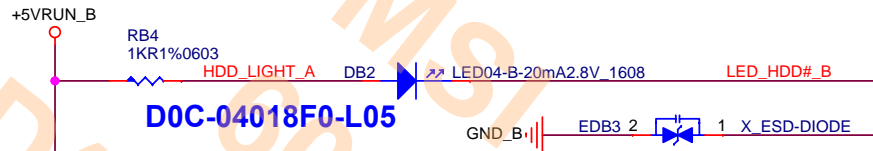
MYLARA1	MYLARA2
E2P-6H22812-G40	E2P-6H22311-G40
MYLAR	MYLAR

msi MICRO-STAR INT'L CO.,LTD.		
Title	[A] USB3.0 CNT-3/4	
Size	Document Number	Rev
	MS-16H8	10
Date:	Tuesday, May 26, 2015	Sheet 56 of 63

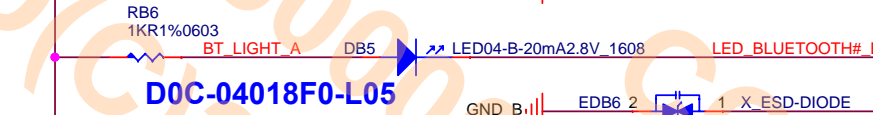
16H8B Board (LED Board)

LED

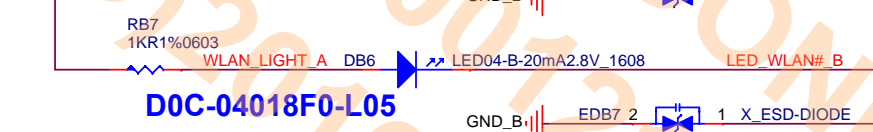
BLUE
(HDD)



BLUE
(BT)



BLUE
(WLAN)



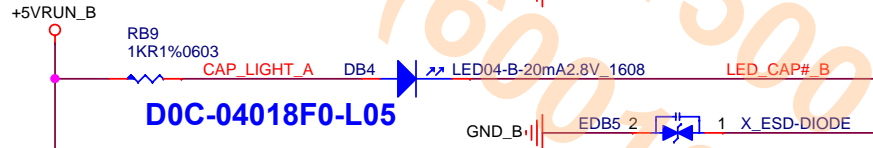
ORANGE
(BATLOW)



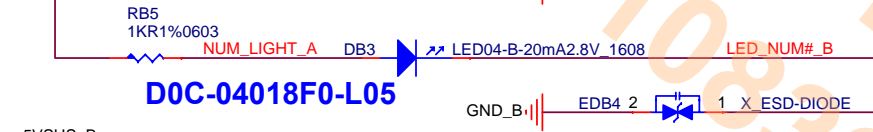
BLUE
(CHARGE)



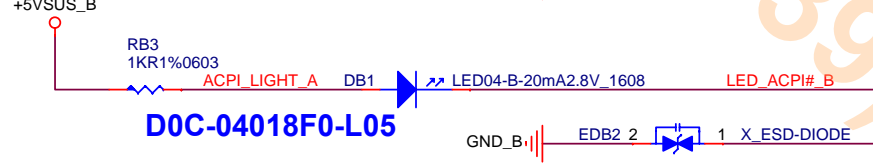
BLUE
(CAP)



BLUE
(NUM)



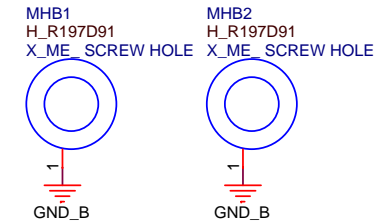
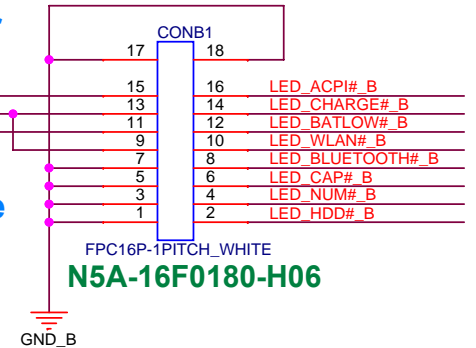
BLUE
(ACPI)



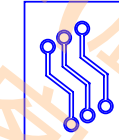
Connector

+5VALW_B
+5VRUN_B
+5VSUS_B

Same Side



PCBB1

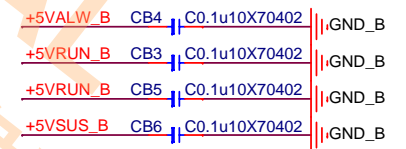


PF0-16H8B0A-H73

PF0-16H8B0A-H73

Hannstar: PF0-16H8B0A-H73

TRIPOD: PF0-16H8B0A-T53



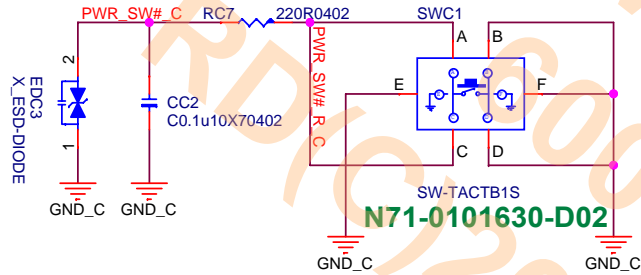
msi

MICRO-STAR INT'L CO.,LTD.

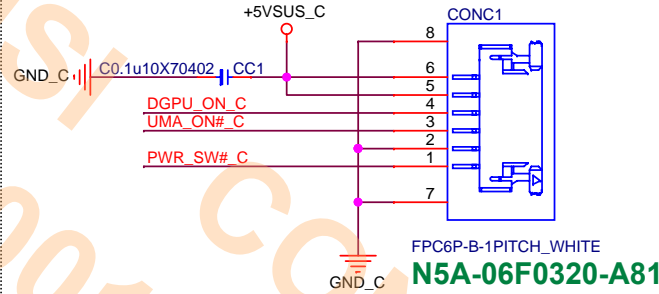
Title		
LED Board		
Size	Document Number	Rev
	MS-16H8	10
Date:	Tuesday, May 26, 2015	Sheet 57 of 63

16H8C Board (Power SW Board)

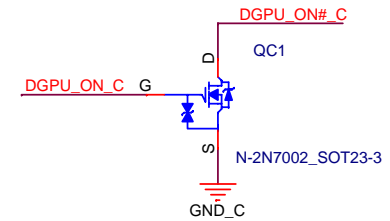
Power Switch



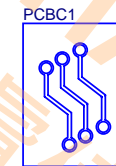
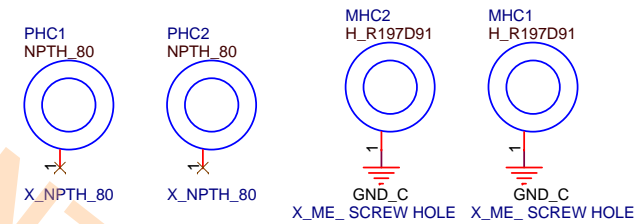
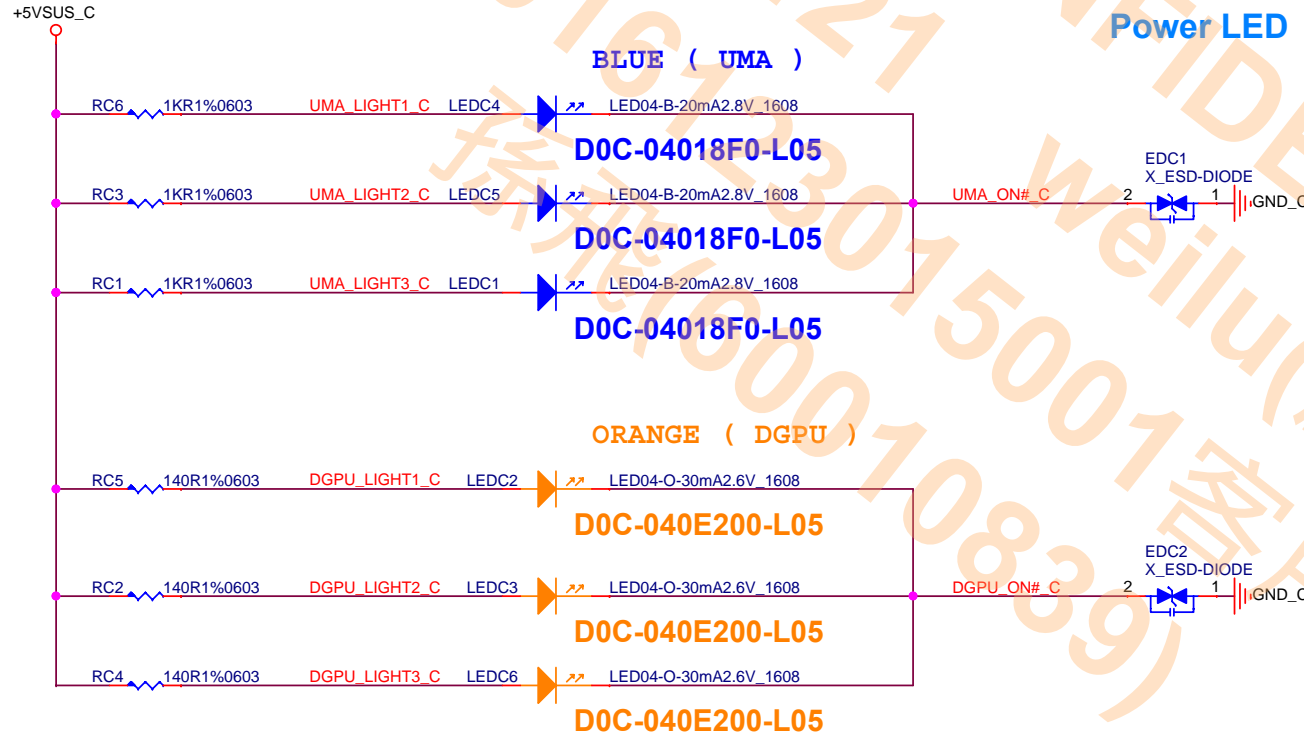
Diff Side Connector



DGPU Logic



Power LED



PF0-16H8C0A-H73

PF0-16H8C0A-H73

Hannstar: PF0-16H8C0A-H73

TRIPOD: PF0-16H8C0A-T53

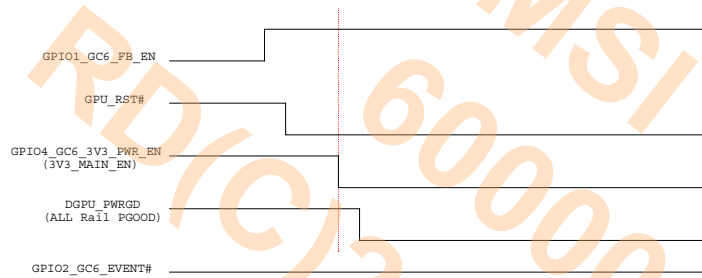


MICRO-STAR INT'L CO.,LTD.

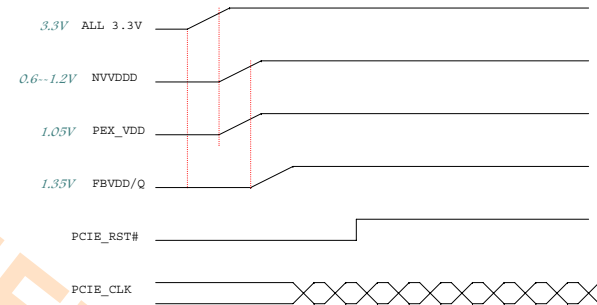
Title			Power SW Board	
Size	Document Number			Rev
	MS-16H8			10
Date:	Monday, May 25, 2015			Sheet 58 of 63

MS-16H8 DGPU POWER SEQUENCE

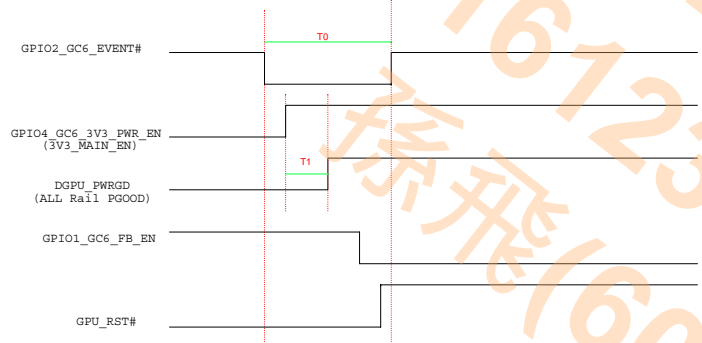
GC6 2.0 ENTRY SEQUENCE



GPU POWER ON SEQUENCE



GC6 2.0 EXIT SEQUENCE



NOTES:

1. The ramp time for any rail must be more than 40 us and is recommended to be less than 2ms.
2. The ramp up overshoot should not exceed the silicon reliability limit voltage.
3. A VDD33 must ramp up to 90% before NVVDD and PEX_VDD in sequence can ramping up. NVVDD must ramp up to 90% before FBVDD/Q in sequence can ramping up.
3. No signal should be applied to the GPU before the power rails are fully ramped.
4. Refer to JEDEC Memory Specification for memory related power sequencing.

GC6 2.0 TIMING

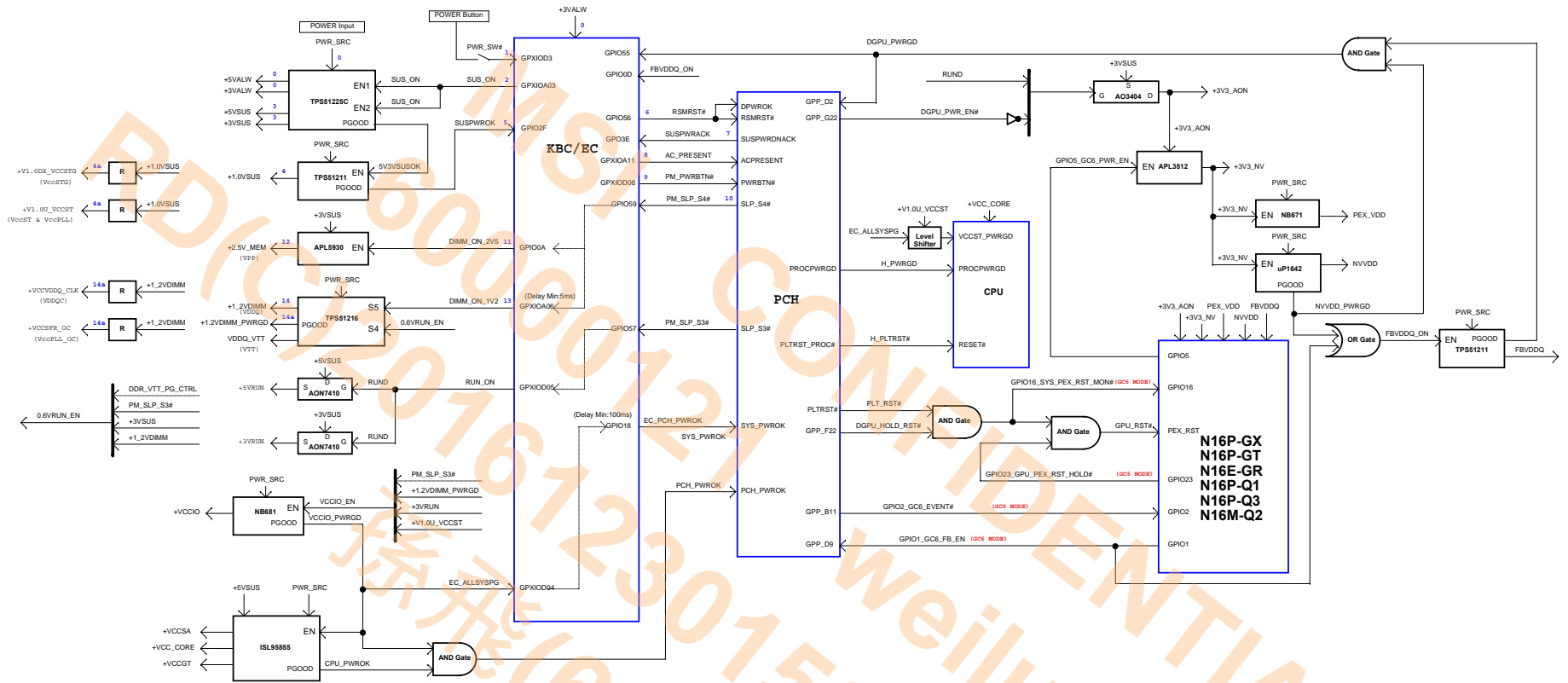
	Min	Max	Unit	Description
T0	0.001	N/A	ms	GPU_EVENT# assertion
T1	0.04	4	ms	3V3_MAIN_EN assertion to all power rails up and stable

NOTES:

1. ALL RailPGOOD=1 represents all GPU power rails are ramped up and in regulation. If any GPU power rail cannot be guaranteed in regulation this state should equal to 0.
2. During GC6 exit, the order of power rail ramp-up must follow the Power up sequence described in Chapter 3 with the exception that FBVDD/Q stays on.
3. All delays should be minimized to increase time spent in GC6 for maximum power saving.
4. The entire entry and exit sequence must complete within 200 ms.

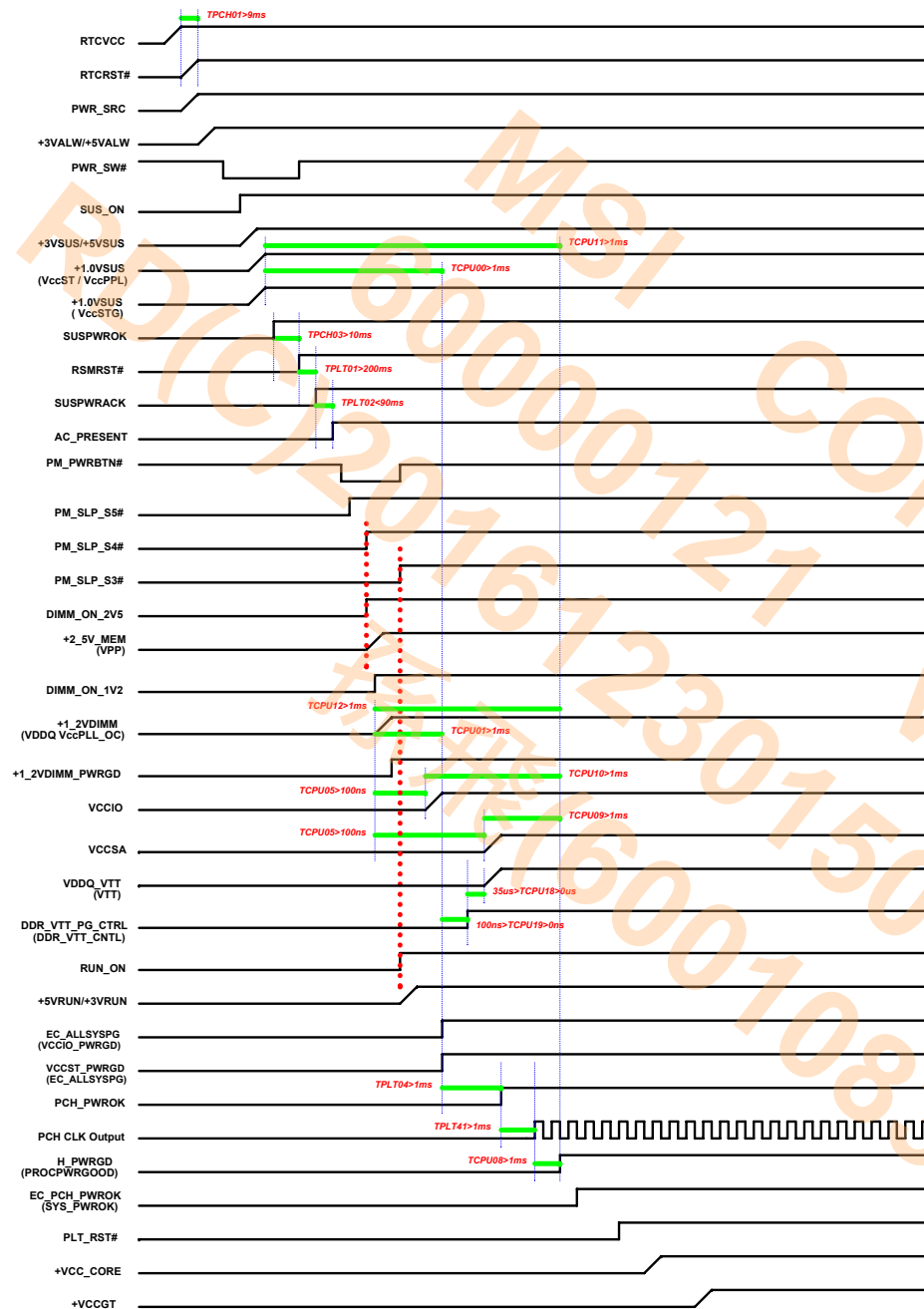
The diagram illustrates the internal components and signal connections of the PCH and CPU. Key elements include:

- PCH (Platform Controller Hub):** A central component with multiple pins (GPIO06, GPIO3E, GPIOA11, GPIOX0D06, GPIO59, GPIOA, GPIOX0A06, GPIO57, GPIOX0D05, GPIO18, GPIOX0D04) and internal logic blocks like RSMRST#, SUSPWACK, AC_PRESENT, PM_PWRSTN#, PM_SLP_S4#, SLP_S3#, EC_PCH_PWROK, SYS_PWROK, PCH_PWROK, PLTRST_PROC#, SLP_S3#, PLTRST#, GPP_F22, GPP_B11, and GPP_D6.
- CPU (Central Processing Unit):** A component with pins (GPP_D2, GPP_G22, DGPU_PWR_EN#, +V1.0U_VCCST, +VCC_CORE, VCCST_PWRGD, PROC_PWRGD, H_PWRGD, H_PLTRST#, RESET#, PLTRST#, DGPU_HOLD_RST#, GPP_D6) and internal logic blocks like Level Shifter, AND Gate, and OR Gate.
- External Components:**
 - APL3512:** A component with pins (GPIO5_G06_PWR_EN, +3V3_AON, +3V3_NV, EN, PWR_SRC, +3V3_NV, NVDD, PGOOD, FBVDDQ, NVVDD_PWRGD, FBVDDQ).
 - NB671:** A component with pins (PWR_SRC, +3V3_NV, NVDD, PGOOD, FBVDDQ, NVVDD_PWRGD, FBVDDQ).
 - uP1642:** A component with pins (PWR_SRC, +3V3_NV, NVDD, PGOOD, FBVDDQ, NVVDD_PWRGD, FBVDDQ).
- Logic Blocks:**
 - Level Shifter:** Translates signals between different voltage levels.
 - AND Gate:** Combines multiple signals to produce a single output.
 - OR Gate:** Combines multiple signals to produce a single output.



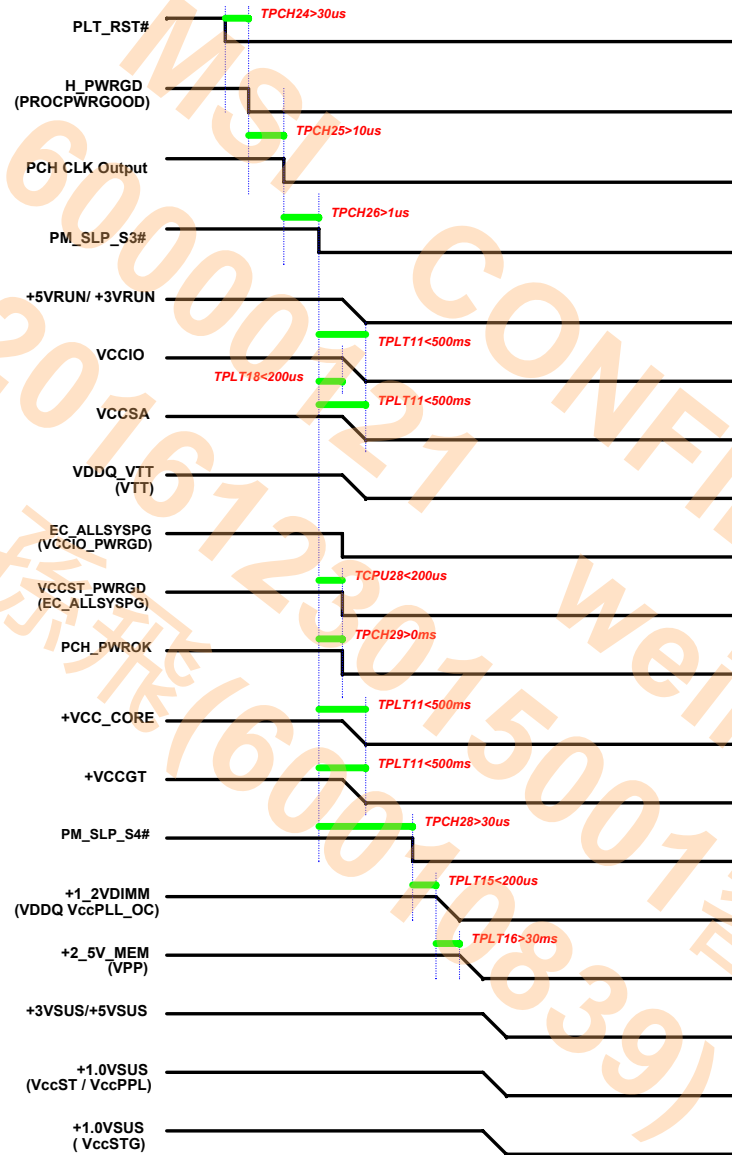
Power On Sequence

G3 -> S0




Power Down Sequence

S0 -> G3



History

MSI CONFIDENTIAL
60000121 weilu(盧偉)
RD(C)2016123015001客戶服務部
孫飛(60010839)

		MICRO-STAR INT'L CO.,LTD.	
Title			
History			
Size	Document Number		Rev
	MS-16H8		10
Date:	Friday, May 22, 2015	Sheet 63 of 63	